Agilent U7231A DDR3 Compliance Test Application

Compliance Testing Notes

Agilent Technologies

Notices

© Agilent Technologies, Inc. 2007-2011

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Agilent Technologies, Inc. as governed by United States and international copyright laws.

Manual Part Number

Manual for software version 01.60.0000 or greater

Edition

Seventh edition, March 2011

Available in electronic format only

Agilent Technologies, Inc.
1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

Warranty

The material contained in this document is provided "as is," and is subject to being changed, without notice, in future editions. Further, to the maximum extent permitted by applicable law, Agilent disclaims all warranties, either express or implied, with regard to this manual and any information contained herein, including but not limited to the implied warranties of merchantability and fitness for a particular purpose. Agilent shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein. Should Agilent and the user have a separate written agreement with warranty terms covering the material in this document that conflict with these terms, the warranty terms in the separate agreement shall control.

Technology Licenses

The hardware and/or software described in this document are furnished under a license and may be used or copied only in accordance with the terms of such license.

Restricted Rights Legend

If software is for use in the performance of a U.S. Government prime contract or subcontract, Software is delivered and licensed as "Commercial computer software" as defined in DFAR 252.227-7014 (June 1995), or as a "commercial item" as defined in FAR 2.101(a) or as "Restricted computer software" as defined in FAR 52.227-19 (June 1987) or any equivalent agency regulation or contract clause. Use, duplication or disclosure of Software is subject to Agilent Technologies' standard commercial license terms, and non-DOD Departments and Agencies of the U.S. Government will receive no greater than Restricted Rights as defined in FAR 52.227-19(c)(1-2) (June 1987). U.S. Government users will receive no greater than Limited Rights as defined in FAR 52.227-14 (June 1987) or DFAR 252.227-7015 (b)(2) (November 1995), as applicable in any technical data.

Safety Notices

CAUTION

A **CAUTION** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a **CAUTION** notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

DDR3 —An Overview

DDR3 SDRAM or double data rate three synchronous dynamic random access memory is a random access memory technology used for high speed storage of the working data of an electronic device. It is an evolutionary improvement over its predecessor, DDR2 SDRAM.

Table 1 General Characteristics and Specifications of DDR3

Component Speed	Module Speed	Data Rate	Memory Clock
DDR3-800	PC3-6400	800 MT/s	100 MHz (10 ns)
DDR3-1066	PC3-8500	1066 MT/s	133 MHz (7.5 ns)
DDR3-1333	PC3-10600	1333 MT/s	166 MHz (6 ns)
DDR3-1600	PC3-12800	1600 MT/s	200 MHz (5 ns)

The DDR3 components are twice as fast as DDR2 memory products. The main advantages of DDR3 are the higher bandwidth and the increase in performance at low power. The DDR3 SDRAM devices offer data transfer rates up to 1600 Mbps. The supply voltage for the memory technology is being reduced from 1.8 volts for DDR2 to just 1.5 volts for DDR3, which promotes longer battery life. The voltage reduction limits the amount of power that is consumed and heat that is generated in connection with the increase in bandwidth.

DDR3 —Quick Reference

Table 2 DDR3 Cycles and Signals

NOTE: 1 = Single Ended probing; 2 = Differential probing; 3 = 2 x Single Ended probing

TEST	Cycle		Based on Test Definition						Required to Perform on Scope						Opt.
	Read	Write	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	CS#
tJIT(per)					√						√[2]				
tJIT(cc)					√						√[2]				
tERR(nper)					√						√[2]				
tCH(avg)					√						√[2]				
tCL(avg)					√						√[2]				
tJIT(duty)					√						√[2]				
tCK(avg)					√						√[2]				
SlewR		√	√	√	√	√	√	√	√[1]	√[1, 2]	√[1]	√[1]	√[1]	√[1]	
SlewF		√	√	√	√	√	√	√	√[1]	√[1, 2]	√[1]	√[1]	√[1]	√[1]	
VIH(ac)		√	√	√	√	√	√	√	√[1]	√[1, 2]	√[1]	√[1]	√[1]	√[1]	
VIH(dc)		√	√	√	√	√	√	√	√[1]	√[1, 2]	√[1]	√[1]	√[1]	√[1]	
VIL(ac)		√	√	√	√	√	√	√	√[1]	√[1, 2]	√[1]	√[1]	√[1]	√[1]	
VIL(dc)		√	√	√	√	√	√	√	√[1]	√[1, 2]	√[1]	√[1]	√[1]	√[1]	
SRQseR	√		√	√					√[1]	√[1, 2]					
SRQseF	√		√	√					√[1]	√[1, 2]					
VOH(ac)	√		√	√					√[1]	√[1, 2]					
VOH(dc)	√		√	√					√[1]	√[1, 2]					
VOL(ac)	√		√	√					√[1]	√[1, 2]					
VOL(dc)	√		√	√					√[1]	√[1, 2]					
AC Overshoot			√	√	√	√	√	√	√[1]	√[1]	√[1]	√[1]	√[1]	√[1]	
AC Undershoot			√	√	√	√	√	√	√[1]	√[1]	√[1]	√[1]	√[1]	√[1]	
VIX(ac)		√		√	√					√[3]	√[3]				

Table 2 DDR3 Cycles and Signals

NOTE: 1 = Single Ended probing; 2 = Differential probing; 3 = 2 x Single Ended probing

TEST	Cycle		Based on Test Definition						Required to Perform on Scope						Opt.
	Read	Write	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	CS#
Eye Diagram - Read	√		√	√					√[1]	√[2]					
Eye Diagram - Write		√	√	√					√[1]	√[2]					
tDQSCK	√			√	√				√[1]	√[2]	√[2]				√
tHZ(DQ)	√		√		√				√[1]	√[2]	√[2]				√
tLZ(DQS)	√			√	√				√[1]	√[2]	√[2]				√
tLZ(DQ)	√		√		√				√[1]	√[2]	√[2]				√
tDQSQ	√		√	√					√[1]	√[2]	√[2]				√
tQH	√		√	√					√[1]	√[2]	√[2]				√
tDQSS		√		√	√				√[1]	√[2]	√[2]				√
tDQSH		√		√					√[1]	√[2]	√[2]				√
tDQSL		√		√					√[1]	√[2]	√[2]				√
tDSS		√		√	√				√[1]	√[2]	√[2]				√
tDSH		√		√	√				√[1]	√[2]	√[2]				√
tWPST		√		√					√[1]	√[2]	√[2]				√
tWPRE		√		√					√[1]	√[2]	√[2]				√
tRPRE	√			√					√[1]	√[2]	√[2]				√
tRPST	√			√					√[1]	√[2]	√[2]				√
tDS(base)		√	√						√[1]	√[2]	√[2]				√
tDH(base)		√	√						√[1]	√[2]	√[2]				√
tDS(derate)		√	√						√[1]	√[2]	√[2]				√
tDH(derate)		√	√						√[1]	√[2]	√[2]				√
tIS(base)		√			√	√	√				√[2]	√[1]	√[1]		√
tIH(base)		√			√	√	√				√[2]	√[1]	√[1]		√
tIS(derate)		√			√	√	√				√[2]	√[1]	√[1]		√
tIH(derate)		√			√	√	√				√[2]	√[1]	√[1]		√

DDR3 Compliance Test Application — At A Glance

The Agilent U7231A DDR3 Compliance Test Application is a DDR3 (Double Data Rate 3) test solution that covers electrical, clock and timing parameters of the JEDEC (Joint Electronic Device Engineering Council) specifications, specifically *JESD79-3*. The software helps you in testing all the un-buffered DDR3 device under test (DUT) compliance, with the Agilent 9000, 80000, or 90000A Series Infiniium digital storage oscilloscope.

There are 2 main categories of test modes:

- Compliance Tests - These tests are based on the DDR3 JEDEC compliance specifications and are compared to corresponding compliance test limits.
- Custom Tests - These tests are not based on any compliance specification. The primary use of these tests is to perform signal debugging.

The DDR3 Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Allows you to determine the number of trials for each test, with the new multi trial run capability.
- Provides detailed information of each test that has been run. The result of maximum twenty five worst trials can be displayed at any one time.
- Creates a printable HTML report of the tests that have been run.

The minimum number of probes required for the tests are:

- Clock tests - 1 probe.
- Electrical tests - 3 probes.
- Clock Timing tests - 3 probes.
- Custom tests - 3 probes.

NOTE The tests performed by the DDR3 Compliance Test Application are intended to provide a quick check of the physical layer performance of the DUT. These testing are not replacement for an exhaustive test validation plan.

DDR3 SDRAM electrical, clock and timing test standards and specifications are described in the *JESD79-3* document. For more information, please refer to JEDEC web site at www.jedec.org.

Required Equipment and Software

In order to run the DDR3 automated tests, you need the following equipment and software:

- 9000, 80000B or 90000A Series Infiniium Digital Storage Oscilloscope. Agilent recommends using 4 GHz and higher bandwidth oscilloscope.
- Infiniium software revision 05.71 (80000 Series) / revision 2.10 (9000, 90000 Series) or later.
- U7231A DDR3 Compliance Test Application.
- RAM reliability test software.
- 1169A, 1168A, 1134A, 1132A or 1131A InfiniiMax probe amplifiers.
- N5381A or E2677A differential solder-in probe head, N5382A or E2675A differential browser probe head, N5425A ZIF probe head or N5426A ZIF tips, E2678A differential socketed probe head.
- Any computer motherboard system that supports DDR3 memory.
- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).

Below are the required licenses:

- U7231A DDR3 Compliance Test Application license.
- N5414A InfiniiScan software license. (90000A and 80000 Series)
- N5415A InfiniiScan software license. (9000 Series)
- E2688A Serial Data Analysis and Clock Recovery software license.

In This Book

This manual describes the tests that are performed by the DDR3 Compliance Test Application in more detail; it contains information from (and refers to) the *JESD79-3*, and it describes how the tests are performed.

- Chapter 1, “Installing the DDR3 Compliance Test Application” shows how to install and license the automated test application software (if it was purchased separately).
- Chapter 2, “Preparing to Take Measurements” shows how to start the DDR3 Compliance Test Application and gives a brief overview of how it is used.
- Chapter 3, “Measurement Clock Tests” describes the measurement clock tests including clock period jitter, clock to clock period jitter, cumulative error, average high and low pulse width, half period jitter and average clock period tests.
- Chapter 3, “Single-Ended Signals AC Input Parameters Tests” shows how to run the single-ended signals AC input parameters tests. This chapter includes input signal maximum peak to peak swing tests, input signal minimum slew rate (rising) tests, input signal minimum slew rate (falling) tests, input logic high tests and input logic low tests.
- Chapter 4, “Single-Ended Signals AC Output Parameters Tests” shows how to run the single-ended signals AC output parameters tests.
- Chapter 5, “Single-Ended Signals Overshoot/Undershoot Tests” describes the AC overshoot and undershoot tests probing and method of implementation.
- Chapter 6, “Differential Signals AC Input Parameters Tests” describes the V_{IX} AC differential cross point voltage tests.
- Chapter 7, “Clock Timing (CT) Tests” describes the clock timing operating conditions of DDR3 SDRAM as defined in the specification.
- Chapter 8, “Data Strobe Timing (DST) Tests” describes various data strobe timing tests including tHZ(DQ), tLZ(DQS), tLZ(DQ), tDQSQ, tQH, tDQSS, tDQSH, tDQSL, tDSS, tDSH, tWPST, tWPRE, tRPRE and tRPST tests.
- Chapter 9, “Data Timing (DT) Tests” describes the data mask timing tests including tDS(base) and tDH(base) tests.
- Chapter 10, “Command and Address Timing (CAT) Tests” describes the command and address timing tests including address and control input setup time as well as address and control input hold time.
- Chapter 11, “Custom Mode Read-Write Eye-Diagram Tests” describes the user defined real-time eye-diagram test for read cycle and write cycle.

- Chapter 12, “Calibrating the Infiniium Oscilloscope and Probe” describes how to calibrate the oscilloscope in preparation for running the DDR3 automated tests.
- Chapter 13, “InfiniiMax Probing” describes the probe amplifier and probe head recommendations for DDR3 testing.

See Also

- The DDR3 Compliance Test Application’s online help, which describes:
  - Starting the DDR3 compliance test application.
  - Creating or opening a test project.
  - Setting up DDR3 test environment.
  - Selecting tests.
  - Configuring selected tests.
  - Connecting the oscilloscope to the DUT.
  - Running tests.
  - Viewing test results.
  - Viewing/printing the HTML test report.
  - Understanding the HTML report.
  - Saving test projects.

Contact Agilent

For more information on DDR3 Compliance Test Application or other Agilent Technologies' products, applications and services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Phone or Fax

United States:

(tel) 800 829 4444

(fax) 800 829 4433

Canada:

(tel) 877 894 4414

(fax) 800 746 4866

China:

(tel) 800 810 0189

(fax) 800 820 2816

Europe:

(tel) 31 20 547 2111

Japan:

(tel) (81) 426 56 7832

(fax) (81) 426 56 7840

Korea:

(tel) (080) 769 0800

(fax) (080) 769 0900

Latin America:

(tel) (305) 269 7500

Taiwan:

(tel) 0800 047 866

(fax) 0800 286 331

Other Asia Pacific Countries:

(tel) (65) 6375 8100

(fax) (65) 6755 0042

E-mail: tm_ap@agilent.com

Contents

DDR3 —An Overview 3

DDR3 —Quick Reference 4

DDR3 Compliance Test Application — At A Glance 6
- Required Equipment and Software 7

In This Book 8
- See Also 9

Contact Agilent 10
- Phone or Fax 10

1 Installing the DDR3 Compliance Test Application

Installing the Software 21

Installing the License Key 21

2 Preparing to Take Measurements

Calibrating the Oscilloscope 24

Starting the DDR3 Compliance Test Application 25
- Online Help Topics 26

3 Single-Ended Signals AC Input Parameters Tests

Probing for Single-Ended Signals AC Input Parameters Tests 30
- Test Procedure 31

SlewR Test Method of Implementation 33
- Signals of Interest 33
- Test Definition Notes 34
- PASS Condition 34
- Measurement Algorithm 34

SlewF Test Method of Implementation 36
- Signals of Interest 36
- Test Definition Notes 37
- PASS Condition 37
- Measurement Algorithm 37

VIH(AC) Test Method of Implementation 39
Signals of Interest 39
Test Definition Notes from the Specification 40
Test References 40
PASS Condition 40
Measurement Algorithm (if PUT is DQ or DM) 40
Measurement Algorithm (if PUT is anything other than DQ or DM) 41

VIH(DC) Test Method of Implementation 42
Signals of Interest 42
Test Definition Notes from the Specification 43
Test References 43
PASS Condition 43
Measurement Algorithm (if PUT is DQ or DM) 43
Measurement Algorithm (if PUT is anything other than DQ or DM) 44

VIL(AC) Test Method of Implementation 45
Signals of Interest 45
Test Definition Notes from the Specification 46
Test References 46
PASS Condition 46
Measurement Algorithm (If PUT is DQ or DM) 46
Measurement Algorithm (if PUT is anything other than DQ or DM) 47

VIL(DC) Test Method of Implementation 48
Signals of Interest 48
Test Definition Notes from the Specification 49
Test References 49
PASS Condition 49
Measurement Algorithm (if PUT is DQ or DM) 49
Measurement Algorithm (if PUT is anything other than DQ or DM) 50

4 Single-Ended Signals AC Output Parameters Tests

Probing for Single-Ended Signals AC Output Parameters Tests 52
Test Procedure 53

SRQseR Test Method of Implementation 55
Signals of Interest 55
Test Definition Notes from the Specification 56
Test References 56
PASS Condition 56
Measurement Algorithm 56

SRQseF Test Method of Implementation 58
Signals of Interest 58
Test Definition Notes from the Specification 59
Test References 59
PASS Condition 59
Measurement Algorithm 59
VOH(AC) Test Method of Implementation 61
Signals of Interest 61
Test Definition Notes from the Specification 61
Test References 61
PASS Condition 62
Measurement Algorithm 62
VOH(DC) Test Method of Implementation 63
Signals of Interest 63
Test Definition Notes from the Specification 63
Test References 63
PASS Condition 63
Measurement Algorithm 64
VOL(AC) Test Method of Implementation 65
Signals of Interest 65
Test Definition Notes from the Specification 65
Test References 65
PASS Condition 66
Measurement Algorithm 66
VOL(DC) Test Method of Implementation 67
Signals of Interest 67
Test Definition Notes from the Specification 67
Test References 67
PASS Condition 67
Measurement Algorithm 68
5 Single-Ended Signals Overshoot/Undershoot Tests
Probing for Overshoot/Undershoot Tests 70
Test Procedure 71

AC Overshoot Test Method of Implementation 73
Signals of Interest 73
Test Definition Notes from the Specification 74
Test References 74
PASS Condition 74
Measurement Algorithm 74
AC Undershoot Test Method of Implementation 76
Signals of Interest 76
Test Definition Notes from the Specification 77
Test References 77
PASS Condition 77
Measurement Algorithm 77

6 Differential Signals AC Input Parameters Tests

Probing for Differential Signals AC Input Parameters Tests 80
Test Procedure 81
VIX(AC), AC Differential Input Cross Point Voltage -Test Method of Implementation 83
Signals of Interest 83
Test Definition Notes from the Specification 84
Test References 84
PASS Condition 84
Measurement Algorithm 84

7 Clock Timing (CT) Tests

Probing for Clock Timing Tests 88
Test Procedure 89
Clock Period Jitter - tJIT(per) - Test Method of Implementation 90
Signals of Interest 90
Test Definition Notes from the Specification 90
Pass Condition 90
Measurement Algorithm 90
Test References 91
Cycle to Cycle Period Jitter - tJIT(cc) - Test Method of Implementation 92
Signals of Interest 92
Test Definition Notes from the Specification 92
Pass Condition 92
Measurement Algorithm 93
Test References 93

Cumulative Error - tERR(nper) - Test Method of Implementation 94
Signals of Interest 94
Test Definition Notes from the Specification 95
Pass Condition 95
Measurement Algorithm 95
Test References 96
Average High Pulse Width - tCH(avg) - Test Method of Implementation 97
Signals of Interest 97
Test Definition Notes from the Specification 97
Pass Condition 97
Measurement Algorithm 97
Test References 98
Average Low Pulse Width - tCL(avg) - Test Method of Implementation 99
Signals of Interest 99
Test Definition Notes from the Specification 99
Pass Condition 99
Measurement Algorithm 99
Test References 100
Half Period Jitter - tJIT(duty) - Test Method of Implementation 101
Signals of Interest 101
Test Definition Notes from the Specification 101
Pass Condition 101
Measurement Algorithm 102
Test References 102
Average Clock Period - tCK(avg) - Test Method of Implementation 103
Signals of Interest 103
Test Definition Notes from the Specification 104
Pass Condition 104
Measurement Algorithm 105
Test References 105

8 Data Strobe Timing (DST) Tests

Probing for Data Strobe Timing Tests 108
Test Procedure 109

tDQSCK, DQS Output Access Time from CK/CK #- Test Method of Implementation 110
Signals of Interest 110
Test Definition Notes from the Specification 111
PASS Condition 111
Measurement Algorithm 111
Test References 111

tLZ(DQS), DQS Low-Impedance Time from CK/CK# - Test Method of Implementation 112
Signals of Interest 112
Test Definition Notes from the Specification 113
PASS Condition 113
Measurement Algorithm 113
Test References 113

tDQSS, DQS Latching Transition to Associated Clock Edge - Test Method of Implementation 114
Signals of Interest 114
Test Definition Notes from the Specification 115
PASS Condition 115
Measurement Algorithm 115
Test References 115

tDQSH, DQS Input High Pulse Width - Test Method of Implementation 116
Signals of Interest 116
Test Definition Notes from the Specification 117
PASS Condition 117
Measurement Algorithm 117
Test References 117

tDQSL, DQS Input Low Pulse Width - Test Method of Implementation 118
Signals of Interest 118
Test Definition Notes from the Specification 119
PASS Condition 119
Measurement Algorithm 119
Test References 119

tDSS, DQS Falling Edge to CK Setup Time - Test Method of Implementation 120
Signals of Interest 120
Test Definition Notes from the Specification 121
PASS Condition 121
Measurement Algorithm 121
Test References 122

tDSH, DQS Falling Edge Hold Time from CK - Test Method of Implementation 123
Signals of Interest 123
Test Definition Notes from the Specification 124
PASS Condition 124
Measurement Algorithm 124
Test References 124

tWPST, Write Postamble - Test Method of Implementation 125
Signals of Interest 125
Test Definition Notes from the Specification 126
PASS Condition 126
Measurement Algorithm 126
Test References 126

tWPRE, Write Preamble - Test Method of Implementation 127
Signals of Interest 127
Test Definition Notes from the Specification 128
NOTE 1: Please refer to page 160, *JEDEC Standard JESD79-3*. 128
PASS Condition 128
Measurement Algorithm 128
Test References 128

tRPRE, Read Preamble - Test Method of Implementation 129
Signals of Interest 129
Test Definition Notes from the Specification 130
PASS Condition 130
Measurement Algorithm 130
Test References 130

tRPST, Read Postamble - Test Method of Implementation 131
Signals of Interest 131
Test Definition Notes from the Specification 132
PASS Condition 132
Measurement Algorithm 132
Test References 132

9 Data Timing (DT) Tests

Probing for Data Timing Tests 134
Test Procedure 135

tDS(base), Differential DQ and DM Input Setup Time - Test Method of Implementation 137
Signals of Interest 138
Test Definition Notes from the Specification 138
PASS Condition 138
Measurement Algorithm 139
Test References 139

tDH(base), Differential DQ and DM Input Hold Time - Test Method of Implementation 140
Signals of Interest 141
Test Definition Notes from the Specification 141
PASS Condition 141
Measurement Algorithm 142
Test References 142

tDS-Diff(derate), Differential DQ and DM Input Setup Time with Derating Support - Test Method of Implementation 143
Signals of Interest 143
Test Definition Notes from the Specification 143
PASS Condition 147
Measurement Algorithm 148
Test References 148

tDH-Diff(derate), Differential DQ and DM Input Hold Time with Derating Support - Test Method of Implementation 149
Signals of Interest 149
Test Definition Notes from the Specification 149
PASS Condition 153
Measurement Algorithm 154
Test References 154

tHZ(DQ), DQ Out High Impedance Time From CK/CK# - Test Method of Implementation 155
Signals of Interest 155
Test Definition Notes from the Specification 156
PASS Condition 156
Measurement Algorithm 156
Test References 156

tLZ(DQ), DQ Low-Impedance Time from CK/CK# - Test Method of Implementation 157
Signals of Interest 157
Test Definition Notes from the Specification 158
PASS Condition 158
Measurement Algorithm 158
Test References 158

tDQSQ, DQS-DQ Skew for DQS and Associated DQ Signals - Test Method of Implementation 159
Signals of Interest 159
Test Definition Notes from the Specification 160
PASS Condition 160
Measurement Algorithm 160
Test References 161
tQH, DQ/DQS Output Hold Time From DQS - Test Method of Implementation 162
Signals of Interest 162
Test Definition Notes from the Specification 163
PASS Condition 163
Measurement Algorithm 163
Test References 164
10 Command and Address Timing (CAT) Tests
Probing for Command and Address Timing Tests 166
Test Procedure 167
tIS(base) - Address and Control Input Setup Time - Test Method of Implementation 169
Signals of Interest 170
Test Definition Notes from the Specification 170
PASS Condition 170
Measurement Algorithm 170
Test References 171
tIH(base) - Address and Control Input Hold Time - Test Method of Implementation 172
Signals of Interest 173
Test Definition Notes from the Specification 173
PASS Condition 173
Measurement Algorithm 173
Test References 174
tIS(derate) - Address and Control Input Setup Time with Derating Support - Test Method of Implementation 175
Signals of Interest 175
Test Definition Notes from the Specification 175
PASS Condition 178
Measurement Algorithm 179
Test References 179

tIH(derate) - Address and Control Input Hold Time with Derating Support - Test Method of Implementation 180
Signals of Interest 180
Test Definition Notes from the Specification 180
PASS Condition 183
Measurement Algorithm 184
Test References 184

11 Custom Mode Read-Write Eye-Diagram Tests

Probing for Custom Mode Read-Write Eye Diagram Tests 186
Test Procedure 187

User Defined Real-Time Eye Diagram Test for Read Cycle Method of Implementation 189
Signals of Interest 189
Test References 189
PASS Condition 189
Measurement Algorithm 189

User Defined Real-Time Eye Diagram Test for Write Cycle Method of Implementation 191
Signals of Interest 191
Test References 191
PASS Condition 191
Measurement Algorithm 191

12 Calibrating the Infiniium Oscilloscope and Probe

Required Equipment for Oscilloscope Calibration 193

Internal Calibration 194

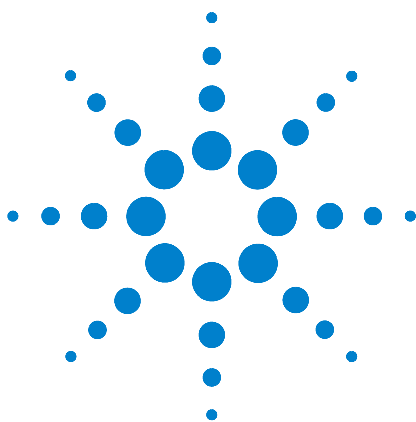
Required Equipment for Probe Calibration 197

Probe Calibration 198
Connecting the Probe for Calibration 198
Verifying the Connection 200
Running the Probe Calibration and Deskew 202

Verifying the Probe Calibration 204

13 InfiniiMax Probing

Index



1
Installing the DDR3 Compliance Test Application

Installing the Software 21
Installing the License Key 21

If you purchased the U7231A DDR3 Compliance Test Application separately, you need to install the software and license key.

Installing the Software

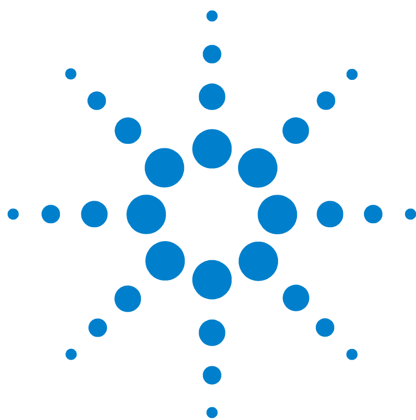
1 Make sure you have version 05.71 (80000 Series) / version 2.10 (9000, 90000 Series) or higher of the Infiniium oscilloscope software by choosing **Help>About Infiniium...** from the main menu.
2 To obtain the DDR3 Compliance Test Application, go to Agilent website: http://www.agilent.com/find/U7231A.
3 The link for DDR3 Compliance Test Application will appear. Double-click on it and follow the instructions to download and install the application software.

Installing the License Key

1 Request a license code from Agilent by following the instructions on the Entitlement Certificate.

   You will need the oscilloscope's "Option ID Number", which you can find in the **Help>About Infiniium...** dialog box.
2 After you receive your license code from Agilent, choose **Utilities>Install Option License...**.
3 In the Install Option License dialog, enter your license code and click **Install License**.
4 Click **OK** in the dialog that tells you to restart the Infiniium oscilloscope application software to complete the license installation.
5 Click **Close** to close the Install Option License dialog.
6 Choose **File>Exit**.

7 Restart the Infiniium oscilloscope application software to complete the license installation.



2
Preparing to Take Measurements

Calibrating the Oscilloscope 24
Starting the DDR3 Compliance Test Application 25

Before running the DDR3 automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this DDR3 application. After the oscilloscope and probe have been calibrated, you are ready to start the DDR3 Compliance Test Application and perform the measurements.

Calibrating the Oscilloscope

If you haven't already calibrated the oscilloscope and probe, see Chapter 12, "Calibrating the Infiniium Oscilloscope and Probe".

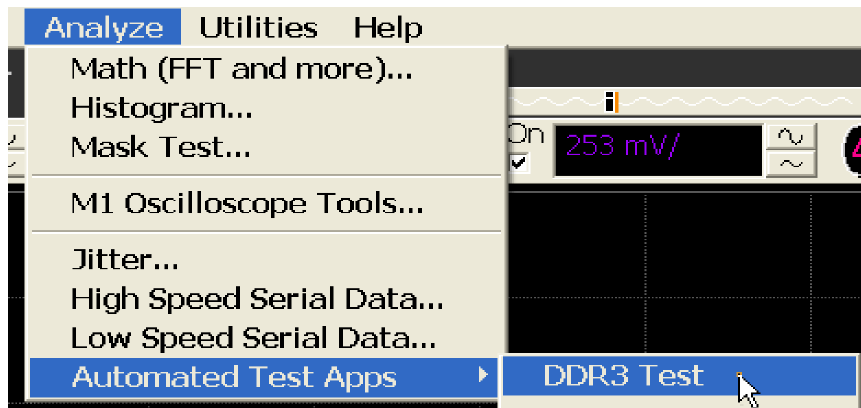
NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Agilent recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the DDR3 Compliance Test Application

1 Ensure that the RAM reliability test software is running in the computer system where the Device Under Test (DUT) is attached. This software performs tests to all unused RAM in the system by producing a repetitive burst of read-write data signals to the DDR3 memory.

2 To start the DDR3 Compliance Test Application: From the Infiniium oscilloscope's main menu, choose **Analyze>Automated Test Apps>DDR3 Test**.



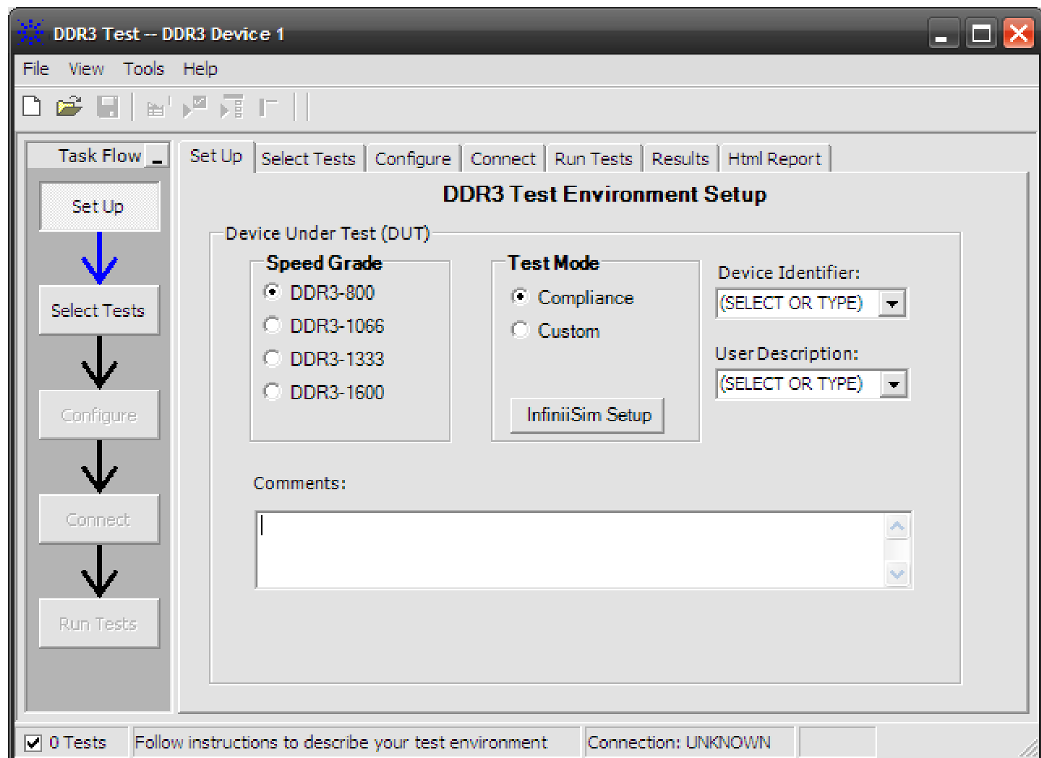


Figure 1 The DDR3 Compliance Test Application

NOTE If DDR3 Test does not appear in the Automated Test Apps menu, the DDR3 Compliance Test Application has not been installed (see Chapter 1, "Installing the DDR3 Compliance Test Application").

Figure 1 shows the DDR3 Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Set Up	Lets you identify and setup the test environment, including information about the device under test.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

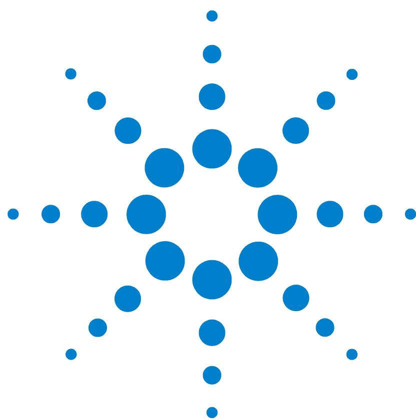
NOTE When you close the DDR3 application, each channel's probe is configured as single-ended or differential depending on the last DDR3 test that was run.

Online Help Topics

For information on using the DDR3 Compliance Test Application, see its online help (which you can access by choosing Help>Contents... from the application's main menu).

The DDR3 Compliance Test Application's online help describes:

- Starting the DDR3 Automated Test Application.
    - To view or minimize the task flow pane.
    - To view or hide the toolbar.
- Creating or opening a test project.
- Setting up DDR3 test environment.
- Selecting tests.
- Configuring selected tests.
- Connecting the oscilloscope to the Device Under Test (DUT).
- Running tests.
- Viewing test results.
    - To show reference images and flash mask hits.
    - To change margin thresholds.
- Viewing/printing the HTML test report.
- Understanding the HTML report.
- Saving test projects.



3
Single-Ended Signals AC Input Parameters Tests

Probing for Single-Ended Signals AC Input Parameters Tests 30
SlewR Test Method of Implementation 33
SlewF Test Method of Implementation 36
VIH(AC) Test Method of Implementation 39
VIH(DC) Test Method of Implementation 42
VIL(AC) Test Method of Implementation 45
VIL(DC) Test Method of Implementation 48

This section provides the Methods of Implementation (MOIs) for Single-Ended Signals AC Input tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Single-Ended Signals AC Input Parameters Tests

When performing the Single-Ended Signals AC Input Parameters tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Single-Ended Signals AC Input Parameters tests may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance application for the exact number of probe connections.

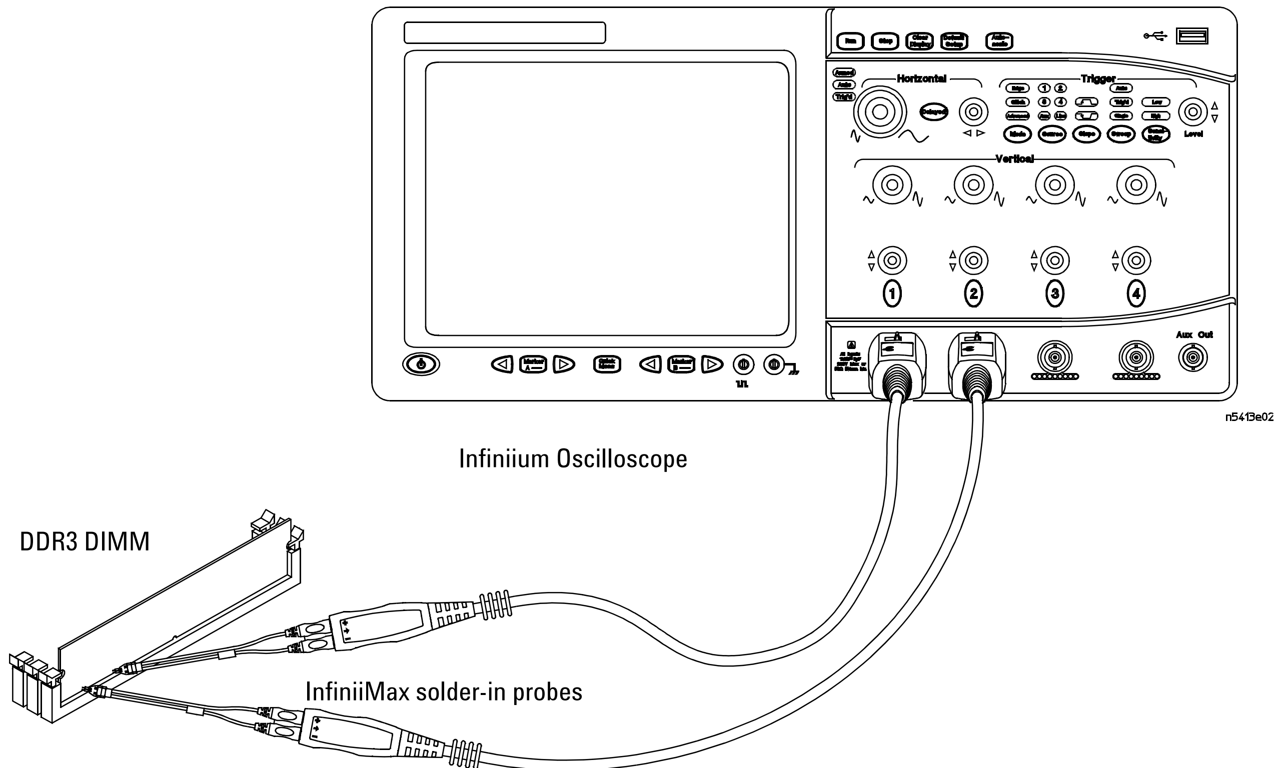


Figure 2 Probing for Single-Ended Signals AC Input Parameters Tests with Two Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 2 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 13, “InfiniiMax Probing,” starting on page 209.

Test Procedure

1 Start the automated test application as described in “Starting the DDR3 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the Set Up tab.

6 Select the Speed Grade options. For the Single-Ended Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

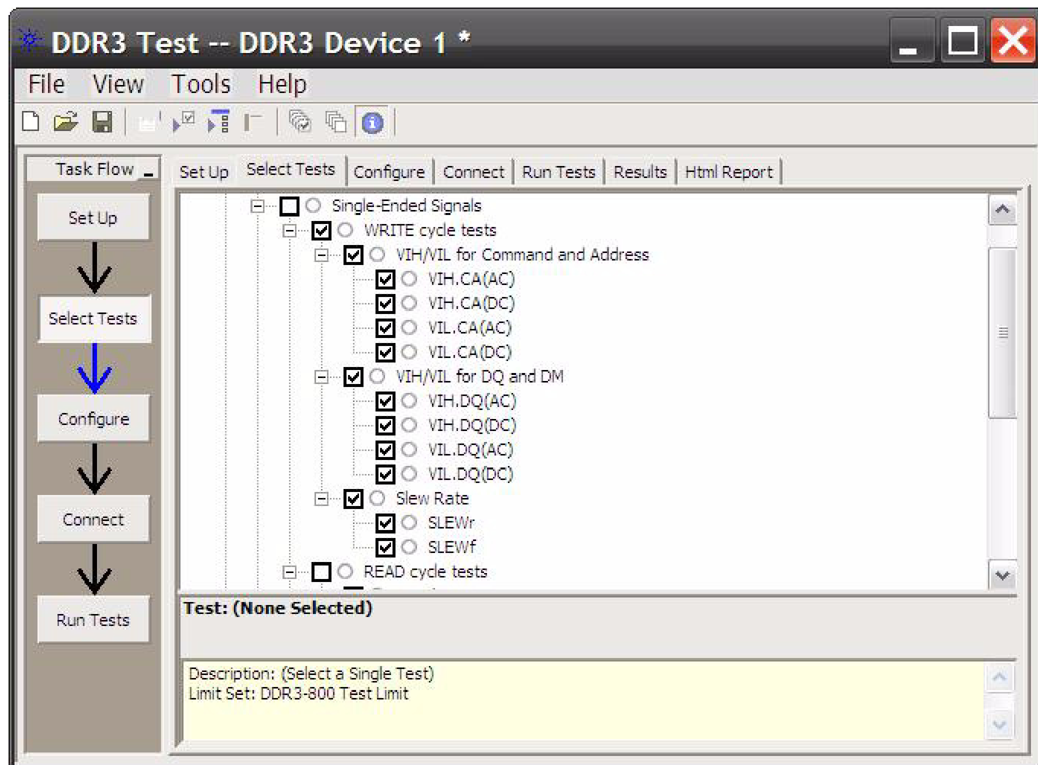


Figure 3 Selecting Single-Ended Signals AC Input Parameters Tests

$Slew_R$ Test Method of Implementation

$Slew_R$ - Input Signal Minimum Slew Rate (Rising). The purpose of this test is to calculate the rising slew rate value of the test signal. The limit is definable by the user for their evaluation tests usage.

This test is only available in custom test mode.

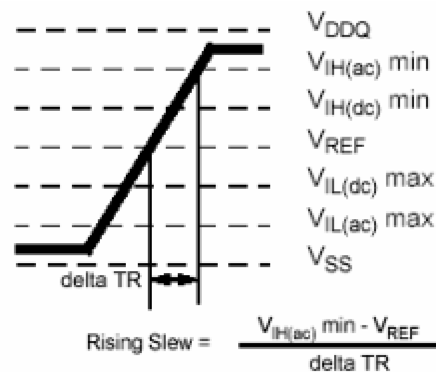


Figure 4 $Slew_R$

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (supported by Data Strobe Signals) OR
- Data Strobe Signal (supported by Data Signals) OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals OR
- Clock Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin (only required when PUT is DQ or DQS)

Test Definition Notes

Table 3 Single-ended Input Slew Rate Definition Test

Description	Measured		Defined by	Applicable for
	from	to		
Input slew rate for rising edge	V_{Ref}	$V_{IH(AC)min}$	$\frac{V_{IH(AC)}min - V_{REF}}{\Delta TRS}$	Setup (t_{IS}, t_{DS})
Input slew rate for falling edge	V_{Ref}	$V_{IL(AC)max}$	$\frac{V_{REF} - V_{IL(AC)max}}{\Delta TFS}$	
Input slew rate for rising edge	$V_{IL(DC)max}$	V_{Ref}	$\frac{V_{REF} - V_{IL(DC)max}}{\Delta TFH}$	Hold (t_{IH}, t_{DH})
Input slew rate for falling edge	$V_{IL(DC)min}$	V_{Ref}	$\frac{V_{IH(DC)}min - V_{REF}}{\Delta TRH}$	

PASS Condition

The calculated Rising Slew value for the test signal shall meet the user defined limit.

Measurement Algorithm

For PUT is DQ or DM or DQS:

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising edges in the said burst. A valid rising edge starts at $V_{IL\ (AC)}$ crossing and end at following $V_{IH\ (AC)}$ crossing.
4 For all valid rising edges, find the transition time, ΔTR which is time starts at V_{REF} crossing and end at following $V_{IH\ (AC)}$ crossing. Then calculate Rising Slew.

$$RisingSlew = \frac{V_{IH(AC)}min - V_{REF}}{\Delta TR}$$

5 Determine the worst result from the set of $Slew_R$ measured.

For other PUT:

1 Acquire the signal.
2 Find all valid rising edges in the whole acquisition. A valid rising edge starts at $V_{IL\ (AC)}$ crossing and end at following $V_{IH\ (AC)}$ crossing.
3 For all valid rising edges, find the transition time, ΔTR which is time starts at V_{REF} crossing and end at following $V_{IH\ (AC)}$ crossing. Then calculate Rising Slew.

$$RisingSlew = \frac{V_{IH(AC)}min - V_{REF}}{\Delta TR}$$

4 Determine the worst result from the set of $Slew_R$ measured.

$Slew_F$ Test Method of Implementation

$Slew_F$ - Input Signal Minimum Slew Rate (Falling). The purpose of this test is to calculate the falling slew rate value of the test signal. The limit is definable by the customers for their evaluation tests usage.

This test is only available in custom test mode.

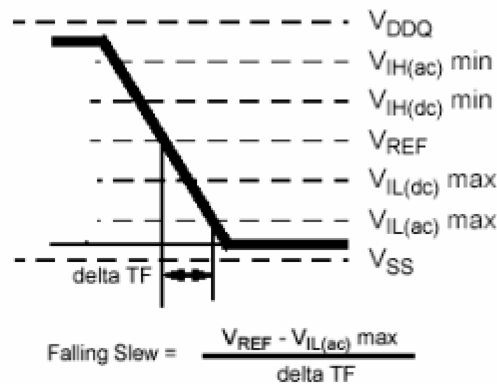


Figure 5 $Slew_F$

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (supported by Data Strobe Signals) OR
- Data Strobe Signal (supported by Data Signals) OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals OR
- Clock Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin (only required when PUT is DQ, or DQS)

Test Definition Notes

Table 4 Single-ended Input Slew Rate Definition Test

Description	Measured		Defined by	Applicable for
	from	to		
Input slew rate for rising edge	V_{Ref}	$V_{IH(AC)min}$	$\frac{V_{IH(AC)}min - V_{REF}}{\Delta TRS}$	Setup (t_{IS}, t_{DS})
Input slew rate for falling edge	V_{Ref}	$V_{IL(AC)max}$	$\frac{V_{REF} - V_{IL(AC)max}}{\Delta TFS}$	
Input slew rate for rising edge	$V_{IL(DC)max}$	V_{Ref}	$\frac{V_{REF} - V_{IL(DC)max}}{\Delta TFH}$	Hold (t_{IH}, t_{DH})
Input slew rate for falling edge	$V_{IL(DC)min}$	V_{Ref}	$\frac{V_{IH(DC)}min - V_{REF}}{\Delta TRH}$	

PASS Condition

The calculated Falling Slew value for the test signal should meet the user defined limit.

Measurement Algorithm

For PUT is DQ or DM or DQS:

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid WRITE burst found.

3 Find all valid falling edges in the said burst. A valid falling edge starts at $V_{IH\ (AC)}$ crossing and end at following $V_{IL\ (AC)}$ crossing.

4 For all valid falling edges, find the transition time, ΔTR which is time starts at V_{REF} crossing and end at following $V_{IL\ (AC)}$ crossing. Then calculate Falling Slew.

$$\text{FallingSlew} = \frac{V_{REF} - V_{IL(ac)}max}{\Delta TF}$$

5 Determine the worst result from the set of $Slew_F$ measured.

For other PUT:

1 Acquire the signal.
2 Find all valid falling edges in the whole acquisition. A valid falling edge starts at $V_{IH\ (AC)}$ crossing and end at following $V_{IL\ (AC)}$ crossing.
3 For all valid falling edges, find the transition time, ΔTR which is time starts at V_{REF} crossing and end at following $V_{IL\ (AC)}$ crossing. Then calculate Falling Slew.

$$\text{FallingSlew} = \frac{V_{REF} - V_{IL(ac)}\text{max}}{\Delta TF}$$

4 Determine the worst result from the set of Slew_F measured.

$V_{IH(AC)}$ Test Method of Implementation

V_{IH} Input Logic High Test can be divided into two sub tests - $V_{IH(AC)}$ test and $V_{IH(DC)}$ test.

$V_{IH(AC)}$:

If PUT (Pin Under Test) is DQ or DM, the purpose of this test is to verify that the voltage level of the test signal at tDS (DM and DQ input setup time in JEDEC specification) with reference to the DQS signal is greater than the conformance lower limits of the $V_{IH(AC)}$ value specified in the JEDEC specification.

If PUT (Pin Under Test) is other than DQ or DM, the purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window is greater than the conformance lower limits of the $V_{IH(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.75V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (supported by Data Strobe Signals) OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals
- Clock Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin (only required when PUT is DQ, DM, or DQS)

Test Definition Notes from the Specification

Table 5 Single Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Units	Notes
		Min	Max		
$V_{IH,CA(AC)}$	AC input logic high	V_{REF} + 0.175	Note 2	V	1, 2

Table 6 Single Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800, DDR3-1066		DDR3-1333, DDR3-1600		Units	Notes
		Min	Max	Min	Max		
$V_{IH,DQ(AC)}$	AC input logic high	V_{REF} + 0.175	Note 2	V_{REF} + 0.150	Note 2	V	1, 2, 5

Test References

See Table 24 - Single Ended AC and DC Input Levels for Command and Address and Table 25 - Single Ended AC and DC Input Levels for DQ and DM, in the *JEDEC Standard JESD79- 3C*.

PASS Condition

$\geq V_{IH\ (AC)}$

If PUT is DQ or DM, the voltage level of the test signal at tDS with reference to the DQS signal should be greater than or equal to the minimum $V_{IH\ (AC)}$ value.

If PUT is other than DQ or DM, the high level voltage value of the test signal within a valid sampling window should be greater than the conformance lower limits of the $V_{IH(AC)}$ value.

Measurement Algorithm (if PUT is DQ or DM)

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising DQ crossings that cross $V_{IH\ (AC)}$ in the said burst.
4. For all DQ crossings found, locate all next DQS crossings that cross 0V.
5. Calculate the time where the test result is taken. Calculation is expressed as $T_{TESTRESULT} = T_{DQS\ MIDPOINT} - tDS$.

(tDS - DM and DQ input setup time in JEDEC specification which due to speed grade.)

6 Take voltage level of DQ signal at $T_{TESTRESULT}$ as the test result for $V_{IH\ (AC)}$.

7 Collect all $V_{IH\ (AC)}$.

8 Determine the worst result from the set of $V_{IH\ (AC)}$ measured.

Measurement Algorithm (if PUT is anything other than DQ or DM)

1 Obtain sample or acquire signal data.

2 Find all valid positive pulses. A valid positive pulse starts at V_{REF} crossing at valid rising edge and ends at V_{REF} crossing at the following valid falling edge.

3 Zoom in on the first valid positive pulse and perform V_{TOP} measurement. Take the V_{TOP} measurement result as $V_{IH.CA\ (AC)}$ value.

4 Continue the previous step with another nine valid positive pulses that were found in the burst.

5 Determine the worst result from the set of $V_{IH.CA\ (AC)}$ measured.

$V_{IH(DC)}$ Test Method of Implementation

$V_{IH(DC)}$ - Minimum DC Input Logic High.

If PUT (Pin Under Test) is DQ or DM, the purpose of this test is to verify that the histogram minimum value of the test signal within the sampling window (from signal tDS to tDH with reference to the DQS signal) is within the conformance limits of the $V_{IH(DC)}$ value specified in the JEDEC specification.

If PUT is anything other than DQ or DM then the purpose of this test is to verify that the histogram mode value of the test signal within a valid sampling window is within the conformance limits of the $V_{IH(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is set to 0.75V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

The value of VDD which directly affect the conformance lower limit is set to 1.50V for the compliance limit set used. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customize test limit set based on different values of VDD.

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (supported by Data Strobe Signals) OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals
- Clock Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin (only required when PUT is DQ, DM, or DQS)

Test Definition Notes from the Specification

Table 7 Single Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Units	Notes
		Min	Max		
$V_{IH,CA(DC)}$	DC input logic high	V_{REF} + 0.100	VDD	V	1

Table 8 Single Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800, DDR3-1066		DDR3-1333, DDR3-1600		Units	Notes
		Min	Max	Min	Max		
$V_{IH,DQ(DC)}$	DC input logic high	V_{REF} + 0.100	VDD	V_{REF} + 0.100	VDD	V	1

Test References

See Table 24 - Single Ended AC and DC Input Levels for Command and Address and Table 25 - Single Ended AC and DC Input Levels for DQ and DM, in the *JEDEC Standard JESD79- 3C*.

PASS Condition

If PUT is DQ or DM, the histogram minimum value of the test signal within the sampling window (from signal tDS to tDH with reference to the DQS signal) should be within the specification limits.

If PUT is other than DQ or DM, the high level voltage value of the test signal shall be greater than or equal to the minimum $V_{IH.CA\ (DC)}$ value.

Measurement Algorithm (if PUT is DQ or DM)

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising DQ crossings that cross $V_{IH\ (AC)}$ in the said burst.
4. For all DQ crossings found, locate all next DQS crossings that cross midpoint. (0V for differential DQS and V_{REF} for single ended DQS.)
5. Setup the histogram function settings.
6. Set the histogram window as follows:
   - Ax: X-time position of tDS (DM and DQ input setup time in JEDEC specification) before DQS crossing midpoint.

- Bx: X-time position of tDH (DM and DQ input hold time in JEDEC specification) after DQS crossing midpoint.
- By: Y-position at V_{REF} voltage level.
- Ay: Top of the displaying window to make sure it covers the maximum level of the respective signal.

7. Use histogram ‘Minimum’ value as the test result for $V_{IH(DC)}$.
8. Collect all $V_{IH\ (DC)}$.
9. Determine the worst result from the set of $V_{IH\ (DC)}$ measured.

Measurement Algorithm (if PUT is anything other than DQ or DM)

1. Obtain sample or acquire signal data.
2. Find all valid positive pulses. A valid positive pulse starts at V_{REF} crossing at valid rising edge and ends at V_{REF} crossing at the following valid falling edge.
3. Zoom in on the first valid positive pulse and perform V_{TOP} measurement. Take the V_{TOP} measurement result as $V_{IH.CA\ (DC)}$ value.
4. Continue the previous step with another nine valid positive pulses that were found in the burst.
5. Determine the worst result from the set of $V_{IH.CA\ (DC)}$ measured.

$V_{IL(AC)}$ Test Method of Implementation

V_{IL} AC Input Logic Low High Test can be divided into two sub tests: $V_{IL(AC)}$ test and $V_{IL(DC)}$ test.

$V_{IL(AC)}$:

If PUT is DQ or DM then the purpose of this test is to verify that the voltage level of the test signal at tDS (DM and DQ input setup time in JEDEC specification) with reference to the DQS signal is lower than the conformance lower limits of the $V_{IL(AC)}$ value specified in the JEDEC specification.

If PUT is other than DQ or DM, the purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window is lower than the conformance lower limits of the $V_{IL(AC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is defaulted to 0.75 V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (supported by Data Strobe Signals) OR
- Data Strobe Signal (supported by Data Signals) OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin (only required when PUT is DQ, DM, or DQS)

Test Definition Notes from the Specification

Table 9 Single Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Units	Notes
		Min	Max		
$V_{IL,CA(AC)}$	AC input logic low	Note 2	V_{REF} - 0.175	V	1, 2

Table 10 Single Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800, DDR3-1066		DDR3-1333, DDR3-1600		Units	Notes
		Min	Max	Min	Max		
$V_{IL,DQ(AC)}$	AC input logic high	Note 2	V_{REF} -0.175	Note 2	V_{REF} - 0.150	V	1, 2, 5

Test References

See Table 24 - Single Ended AC and DC Input Levels for Command and Address and Table 25 - Single Ended AC and DC Input Levels for DQ and DM, in the *JEDEC Standard JESD79- 3C*.

PASS Condition

$\leq V_{IL(AC)}$

If PUT is DQ or DM, the voltage level of the test signal at tDS with reference to the DQS signal should be less than or equal to the maximum $V_{IL(AC)}$ value.

If PUT is anything other than DQ or DM then the histogram mode value of the test signal should be less than or equal to the maximum $V_{IL(AC)}$ value.

Measurement Algorithm (If PUT is DQ or DM)

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid falling DQ crossings that cross $V_{IL\ (AC)}$ in the said burst.
4. For all DQ crossings found, locate all next DQS crossings that cross midpoint. (0V for differential DQS and V_{REF} for single ended DQS.)
5. Calculate the time where the test result is taken. Calculation is expressed as $T_{TESTRESULT} = T_{DQS\ MIDPOINT} - tDS$.
(tDS - DM and DQ input setup time in JEDEC specification which due to speed grade.)

6 Take voltage level of DQ signal at $T_{TESTRESULT}$ as the test result for $V_{IL\ (AC)}$.
7 Collect all $V_{IL\ (AC)}$.
8 Determine the worst result from the set of $V_{IL\ (AC)}$ measured.

Measurement Algorithm (if PUT is anything other than DQ or DM)

1 Obtain sample or acquire signal data.
2 Find all valid negative pulses. A valid negative pulse starts at V_{REF} crossing at valid falling edge and ends at V_{REF} crossing at the following valid rising edge.
3 Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement result as $V_{IL.CA\ (AC)}$ value.
4 Continue the previous step with another nine valid negative pulses.
5 Determine the worst result from the set of $V_{IL.CA\ (AC)}$ measured.

$V_{IL(DC)}$ Test Method of Implementation

$V_{IL(DC)}$ - Maximum DC Input Logic Low.

If PUT is DQ or DM then the purpose of this test is to verify that the histogram maximum value of the test signal within the sampling window (from signal tDS to tDH with reference to the DQS signal) is within the conformance limits of the $V_{IL(DC)}$ value specified in the JEDEC specification.

If the PUT is anything other than DQ or DM, the purpose of this test is to verify that the histogram mode value of the test signal within a valid sampling window is within the conformance limits of the $V_{IL(DC)}$ value specified in the JEDEC specification.

The value of V_{REF} which directly affects the conformance lower limit is defaulted to 0.75 V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customized test limit set based on different values of V_{REF}.

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (supported by Data Strobe Signals) OR
- Data Strobe Signal (supported by Data Signals) OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals OR
- Clock Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin (only required when PUT is DQ, DM, or DQS)

Test Definition Notes from the Specification

Table 11 Single Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Units	Notes
		Min	Max		
$V_{IL,CA(DC)}$	DC input logic low	VSS	V_{REF} - 0.100	V	1

Table 12 Single Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800, DDR3-1066		DDR3-1333, DDR3-1600		Units	Notes
		Min	Max	Min	Max		
$V_{IH,DQ(DC)}$	DC input logic low	VSS	V_{REF} -0.100	VSS	V_{REF} - 0.100	V	1

Test References

See Table 24 - Single Ended AC and DC Input Levels for Command and Address and Table 25 - Single Ended AC and DC Input Levels for DQ and DM, in the *JEDEC Standard JESD79- 3C*.

PASS Condition

If PUT is DQ or DM, the histogram maximum value of the test signal within the sampling window (from signal tDS to tDH with reference to the DQS signal) should be within the specification limits.

If PUT is other than DQ or DM, the low level voltage value of the test signal shall be less than or equal to the maximum $V_{IL.CA\ (DC)}$ value.

Measurement Algorithm (if PUT is DQ or DM)

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid falling DQ crossings that cross $V_{IL\ (AC)}$ in the said burst.
4. For all DQ crossings found, locate all next DQS crossings that cross midpoint. (0V for differential DQS and V_{REF} for single ended DQS.)
5. Setup the histogram function settings.
6. Set the histogram window as follows:
   - Ax: X-time position of tDS (DM and DQ input setup time in JEDEC specification) before DQS crossing midpoint.

- Bx: X-time position of tDH (DM and DQ input hold time in JEDEC specification) after DQS crossing midpoint.
- By: Y-position at V_{REF} voltage level.
- Ay: Top of the displaying window to make sure it covers the maximum level of the respective signal.

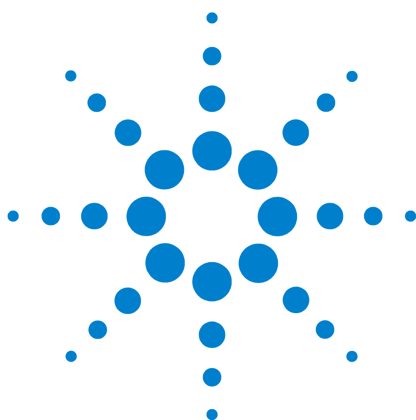
7 Use histogram 'Max' value as the test result for $V_{IL\ (DC)}$.

8 Collect all $V_{IL\ (DC)}$.

9 Determine the worst result from the set of $V_{IL\ (DC)}$ measured.

Measurement Algorithm (if PUT is anything other than DQ or DM)

1. Obtain sample or acquire signal data.
2. Find all valid negative pulses. A valid negative pulse starts at V_{REF} crossing at valid falling edge and ends at V_{REF} crossing at the following valid rising edge.
3. Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement result as $V_{IL.CA\ (AC)}$ value.
4. Continue the previous step with another nine valid negative pulses.
5. Determine the worst result from the set of $V_{IL.CA\ (AC)}$ measured.



4
Single-Ended Signals AC Output Parameters Tests

Probing for Single-Ended Signals AC Output Parameters Tests 52
SRQseR Test Method of Implementation 55
SRQseF Test Method of Implementation 58
VOH(AC) Test Method of Implementation 61
VOH(DC) Test Method of Implementation 63
VOL(AC) Test Method of Implementation 65
VOL(DC) Test Method of Implementation 67

This section provides the Methods of Implementation (MOIs) for Single-Ended Signals AC Output tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Single-Ended Signals AC Output Parameters Tests

When performing the Single-Ended Signals AC Output Parameters tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Single-Ended Signals AC Output Parameters tests may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance application for the exact number of probe connections.

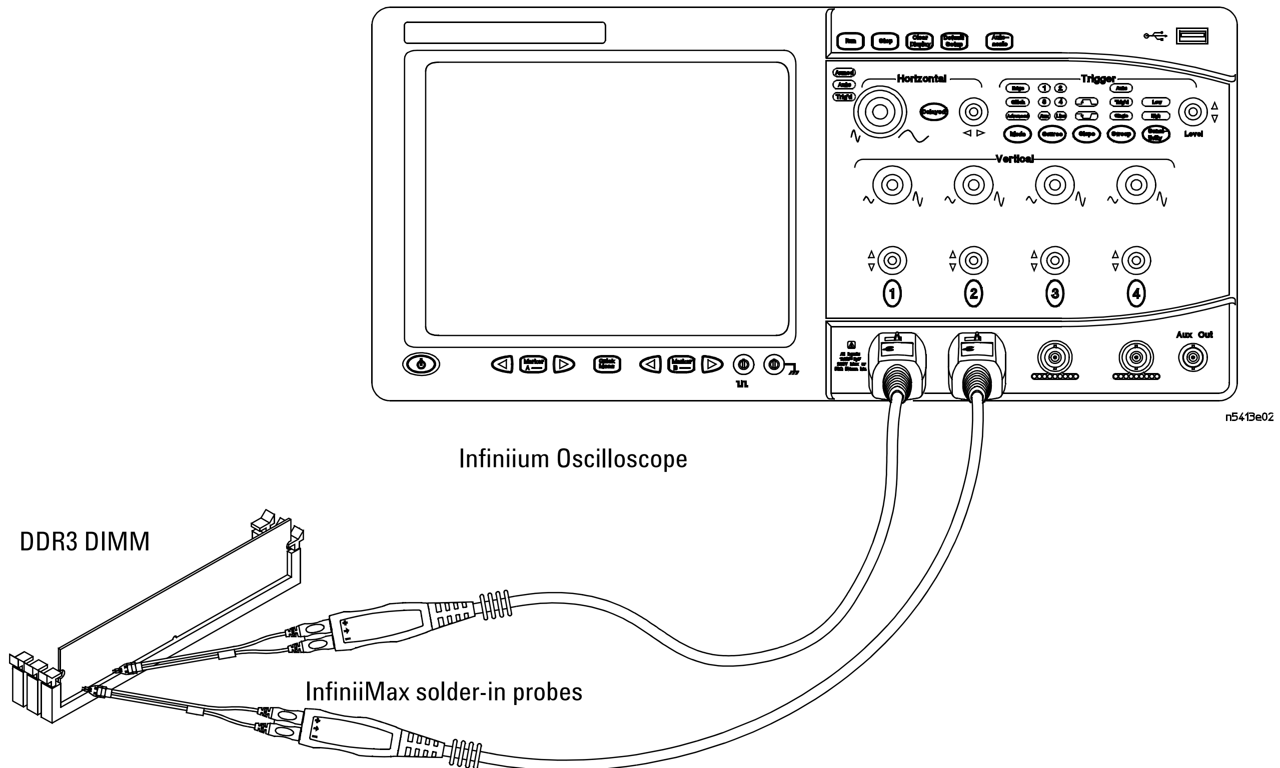


Figure 6 Probing for Single-Ended Signals AC Output Parameters Tests with Two Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 6 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 13, “InfiniiMax Probing,” starting on page 209.

Test Procedure

1 Start the automated test application as described in “Starting the DDR3 Compliance Test Application" on page 25.
2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR3 memory.
3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.
4 Connect the oscilloscope probes to any channels of the oscilloscope.
5 In the DDR3 Test application, click the Set Up tab.
6 Select the Speed Grade options. For the Single-Ended Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.
7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

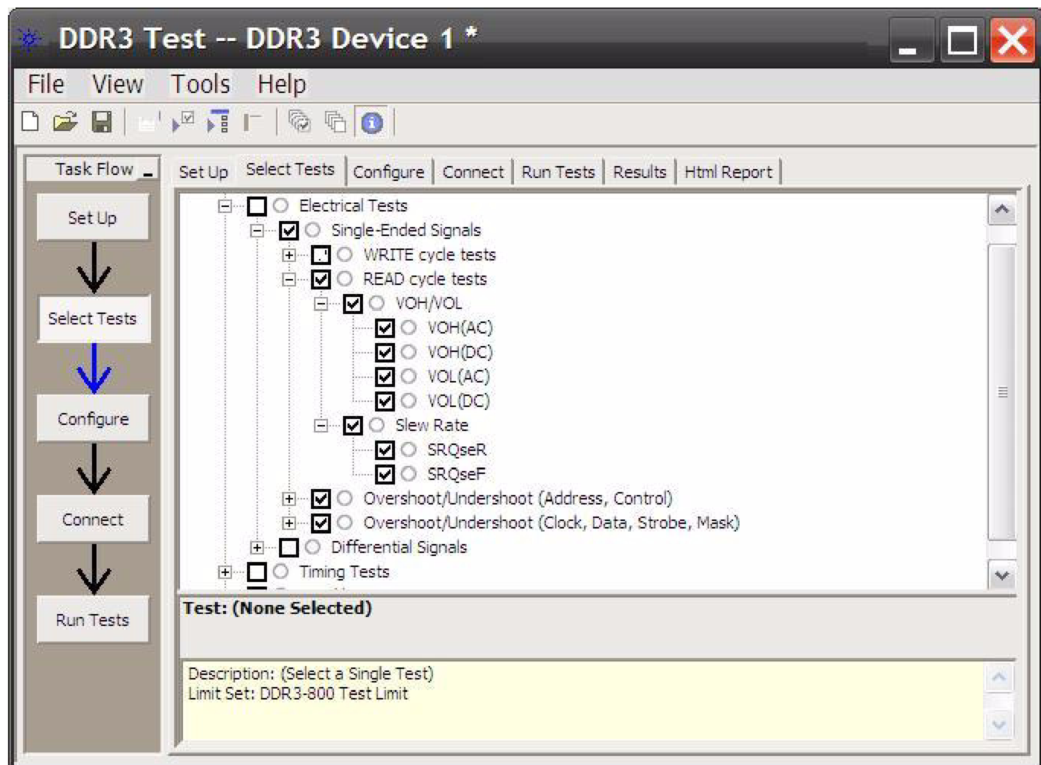


Figure 7 Selecting Single-Ended Signals AC Output Parameters Tests

SRQseR Test Method of Implementation

SRQseR - Output Signal Minimum Rising Slew Rate (Rising). The purpose of this test is to verify that the rising slew rate value of the test signal is within the conformance limit of the SRQser value specified in the JEDEC specification.

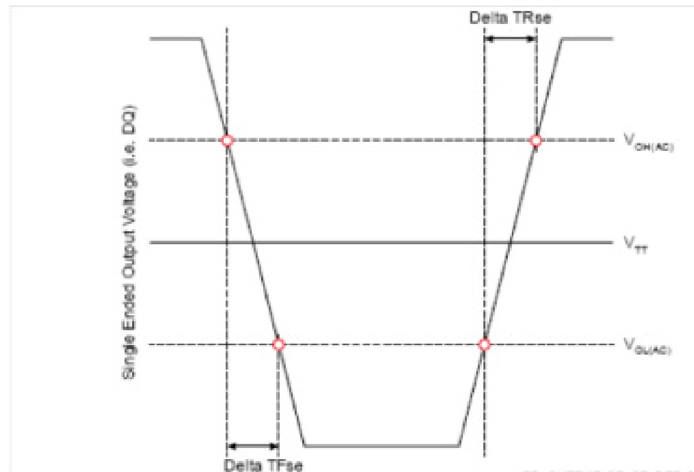


Figure 8 SRQseR

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (supported by Data Strobe Signals) OR
- Data Strobe Signal (supported by Data Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin (only required when PUT is DQ or DQS)

Test Definition Notes from the Specification

Table 13 Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$\frac{V_{OH(AC)}-V_{OL(AC)}}{\Delta TRse}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$\frac{V_{OH(AC)}-V_{OL(AC)}}{\Delta TFse}$
NOTE: Output slew rate is verified by design and characterization, and may not be subject to production test.			

Table 14 Output Slew Rate (Single-Ended)

Parameters	Symbol	DDR3-800		DDR3-1066		DDR3-1333,		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	2.5	5	2.5	5	2.5	5	TBD	5	V/ns
Description: SR: Slew Rate Q: Query Output (like in DQ, which stands for Data-in, Query-Output) se: Single-ended Signals For Ron = RZQ/7 setting										

Test References

See Table 33 - Single-ended Output Slew Rate Definition and Table 34 - Output Slew Rate (Single-ended), in the *JEDEC Standard JESD79-3C*.

PASS Condition

The calculated Rising Slew/SRQseR value for the test signal should be within the specification limit.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid rising edges in the said burst. A valid rising edge starts at $V_{OL\ (AC)}$ crossing and end at following $V_{OH\ (AC)}$ crossing.

4 For all valid rising edges, find the transition time, ΔTR which is time starts at $V_{OL\ (AC)}$ crossing and end at following $V_{OH\ (AC)}$crossing. Then calculate SRQseR.

$$SRQseR = \frac{V_{OH(AC)} - V_{OL(AC)}}{\Delta TR}$$

5 Determine the worst result from the set of SRQseR measured.

SRQseF Test Method of Implementation

SRQseF - Output Signal Minimum Slew Rate (Falling). The purpose of this test is to verify that the falling slew rate value of the test signal is within the conformance limit of the SRQseF value specified in the JEDEC specification.

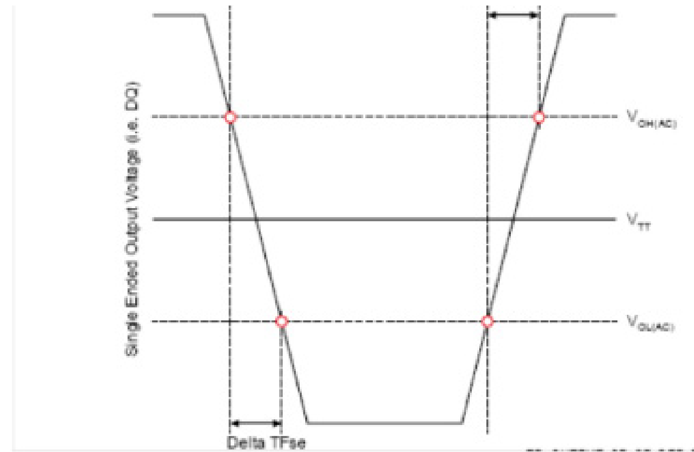


Figure 9 SRQseF

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (supported by Data Strobe Signals) OR
- Data Strobe Signal (supported by Data Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above*
- Supporting Pin (only required when PUT is DQ or DQS)

Test Definition Notes from the Specification

Table 15 Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$\frac{V_{OH(AC)}-V_{OL(AC)}}{\Delta TRse}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$\frac{V_{OH(AC)}-V_{OL(AC)}}{\Delta TFse}$
NOTE: Output slew rate is verified by design and characterization, and may not be subject to production test.			

Table 16 Output Slew Rate (Single-Ended)

Parameters	Symbol	DDR3-800		DDR3-1066		DDR3-1333,		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	2.5	5	2.5	5	2.5	5	TBD	5	V/ns
Description: SR: Slew Rate Q: Query Output (like in DQ, which stands for Data-in, Query-Output) se: Single-ended Signals For Ron = RZQ/7 setting										

Test References

See Table 33 - Single-ended Output Slew Rate Definition and Table 34 - Output Slew Rate (Single-ended), in the *JEDEC Standard JESD79-3C*.

PASS Condition

The calculated Falling Slew/SRQseF value for the test signal should be within the specification limits.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all valid falling edges in the said burst. A valid falling edge starts at $V_{OH\ (AC)}$ crossing and end at following $V_{OL\ (AC)}$ crossing.

4 For all valid falling edges, find the transition time, ΔTR which is time starts at $V_{OH\ (AC)}$ crossing and end at following $V_{OL\ (AC)}$crossing. Then calculate SRQseF.

$$SRQseF = \frac{V_{OH(AC)} - V_{OL(AC)}}{\Delta TR}$$

5 Determine the worst result from the set of SRQseF measured.

$V_{OH(AC)}$ Test Method of Implementation

V_{OH} Output Logic High Test can be divided into two sub tests - $V_{OH(AC)}$ test and $V_{OH(DC)}$ test.

$V_{OH(AC)}$ - Maximum AC Output Logic High. The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window is greater than the conformance limits of the $V_{OH(AC)}$ value specified in the JEDEC specification.

The value of V_{TT} which directly affects the conformance lower limit is defaulted to 0.75V for the compliance limit set used. User may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{TT}.

The value of V_{DDQ} which directly affects the conformance lower limit is defaulted to 1.50V for the compliance limit set used. User may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{TT}.

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal
- Data Strobe Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin (only required when PUT is DQ or DQS)

Test Definition Notes from the Specification

Table 17 Single Ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600	Units	Notes
$V_{OH(AC)}$	AC output logic high measurement level (for output SR)	V_{TT} + 0.1 X V_{DDQ}	V	1
NOTE 1. The swing of ±0.1 x V_{DDQ} is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2.				

Test References

See Table 31 - Single Ended AC and DC Output Levels, in the *JEDEC Standard JESD79- 3C*.

PASS Condition

The high level voltage value of the test signal shall be greater than or equal to the $V_{OH(AC)}$ value in the specification.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid positive pulses. A valid positive pulse starts at V_{REF} crossing at valid rising edge and ends at V_{REF} crossing at the following valid falling edge.
4 Zoom in on the first valid positive pulse and perform V_{TOP} measurement. Take the V_{TOP} measurement result as $V_{OH(AC)}$ value.
5 Continue the previous step with the rest of the valid positive pulses that were found in the burst.
6 Determine the worst result from the set of $V_{OH(AC)}$ measured.

$V_{OH(DC)}$ Test Method of Implementation

$V_{OH(DC)}$ - Minimum DC Output Logic High. The purpose of this test is to verify that the high level voltage value of the test signal within a valid sampling window is greater than the conformance limits of the $V_{OH(DC)}$ value specified in the JEDEC specification.

The value of V_{DDQ} which directly affects the conformance upper limit is defaulted to 1.50V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customize test limit set based on different values of V_{DDQ}.

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (supported by Data Strobe Signals) OR
- Data Strobe Signal (supported by Data Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin (only required when PUT is DQ or DQS)

Test Definition Notes from the Specification

Table 18 Single Ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600	Units
$V_{OH(DC)}$	DC output logic high measurement level (for IV curve linearity)	0.8 X V_{DDQ}	V

Test References

See Table 31 - Single-ended AC and DC Output Levels, in the *JEDEC Standard JESD79-3C*.

PASS Condition

The high level voltage value of the test signal shall be greater than or equal to the $V_{OH(DC)}$ value in the specification.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid positive pulses. A valid positive pulse starts at V_{REF} crossing at valid rising edge and ends at V_{REF} crossing at the following valid falling edge.
4 Zoom in on the first valid positive pulse and perform V_{TOP} measurement. Take the V_{TOP} measurement result as $V_{OH(DC)}$ value.
5 Continue the previous step with the rest of the valid positive pulses that were found in the burst.
6 Determine the worst result from the set of $V_{OH(DC)}$ measured.

$V_{OL(AC)}$ Test Method of Implementation

V_{OL} AC Output Logic Low High Test can be divided into two sub tests: $V_{OL(AC)}$ test and $V_{OL(DC)}$ test.

$V_{OL(AC)}$ - Minimum AC Output Logic Low. The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window is lower than the conformance lower limits of the $V_{OL(AC)}$ value specified in the JEDEC specification.

The value of V_{TT} which directly affects the conformance lower limit is defaulted to 0.75V for the compliance limit set used. User may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{TT}.

The value of V_{DDQ} which directly affects the conformance lower limit is defaulted to 1.50V for the compliance limit set used. User may choose to use the User Defined Limit feature in the application to perform this test against a customized test limit set based on different values of V_{DDQ}.

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (supported by Data Strobe Signals)
- Data Strobe Signal (supported by Data Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin (only required when PUT is DQ or DQS)

Test Definition Notes from the Specification

Table 19 Single Ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600	Units	Notes
$V_{OL(AC)}$	AC output low measurement level (for output SR)	V_{TT} - 0.1 X V_{DDQ}	V	1
NOTE 1. The swing of ±0.1 x V_{DDQ} is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to $V_{TT} = V_{DDQ}/2$.				

Test References

See Table 31 - Single-ended AC and DC Output Levels, in the *JEDEC Standard JESD79-3C*.

PASS Condition

The low level voltage value of the test signal shall be lower than or equal to the minimum $V_{OL(AC)}$ value.

Measurement Algorithm

1 Acquire and split read and write burst of the acquired signal.
2 Take the first valid READ burst found.
3 Find all valid negative pulses. A valid negative pulse starts at V_{REF} crossing at valid falling edge and ends at V_{REF} crossing at the following valid rising edge.
4 Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement result as $V_{OL(AC)}$ value.
5 Continue the previous step with the rest of the valid negative pulses that were found in the burst.
6 Determine the worst result from the set of $V_{OL(AC)}$ measured.

$V_{OL(DC)}$ Test Method of Implementation

$V_{OL(DC)}$ - Maximum DC Output Logic Low. The purpose of this test is to verify that the low level voltage value of the test signal within a valid sampling window is lower than the conformance lower limits of the $V_{OL(DC)}$ value specified in the JEDEC specification.

The value of V_{DDQ} which directly affects the conformance lower limit is defaulted to 1.50V. User may choose to use the UDL (User Defined Limit) feature in the application to perform this test against a customize test limit set based on different values of V_{DDQ}.

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (supported by Data Strobe Signals) OR
- Data Strobe Signal (supported by Data Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin (only required when PUT is DQ or DQS)

Test Definition Notes from the Specification

Table 20 Single Ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600	Units
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 X V_{DDQ}	V

Test References

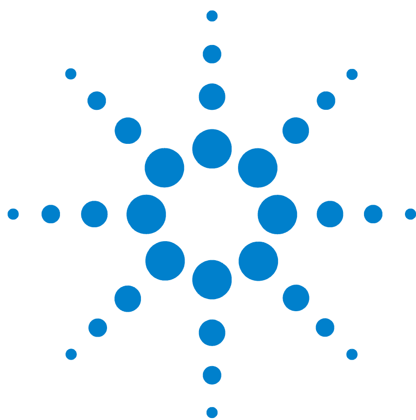
See Table 31 - Single-ended AC and DC Output Levels, in the *JEDEC Standard JESD79-3C*.

PASS Condition

The low level voltage value of the test signal shall be lower than or equal to the minimum $V_{OL(DC)}$ value.

Measurement Algorithm

1. Acquire and split read and write burst of the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid negative pulses. A valid negative pulse starts at V_{REF} crossing at valid falling edge and ends at V_{REF} crossing at the following valid rising edge.
4. Zoom in on the first valid negative pulse and perform V_{BASE} measurement. Take the V_{BASE} measurement result as $V_{OL(DC)}$ value.
5. Continue the previous step with the rest of the valid negative pulses that were found in the burst.
6. Determine the worst result from the set of $V_{OL(DC)}$ measured.



5
Single-Ended Signals Overshoot/Undershoot Tests

Probing for Overshoot/Undershoot Tests 70
AC Overshoot Test Method of Implementation 73
AC Undershoot Test Method of Implementation 76

This section provides the Methods of Implementation (MOIs) for Single-Ended Signals Overshoot/Undershoot tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Overshoot/Undershoot Tests

When performing the Single-Ended Signals Overshoot/Undershoot tests, the DDR3 Compliance Test Application will prompt you to make the proper connections as shown in the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance application for the exact number of probe connections.

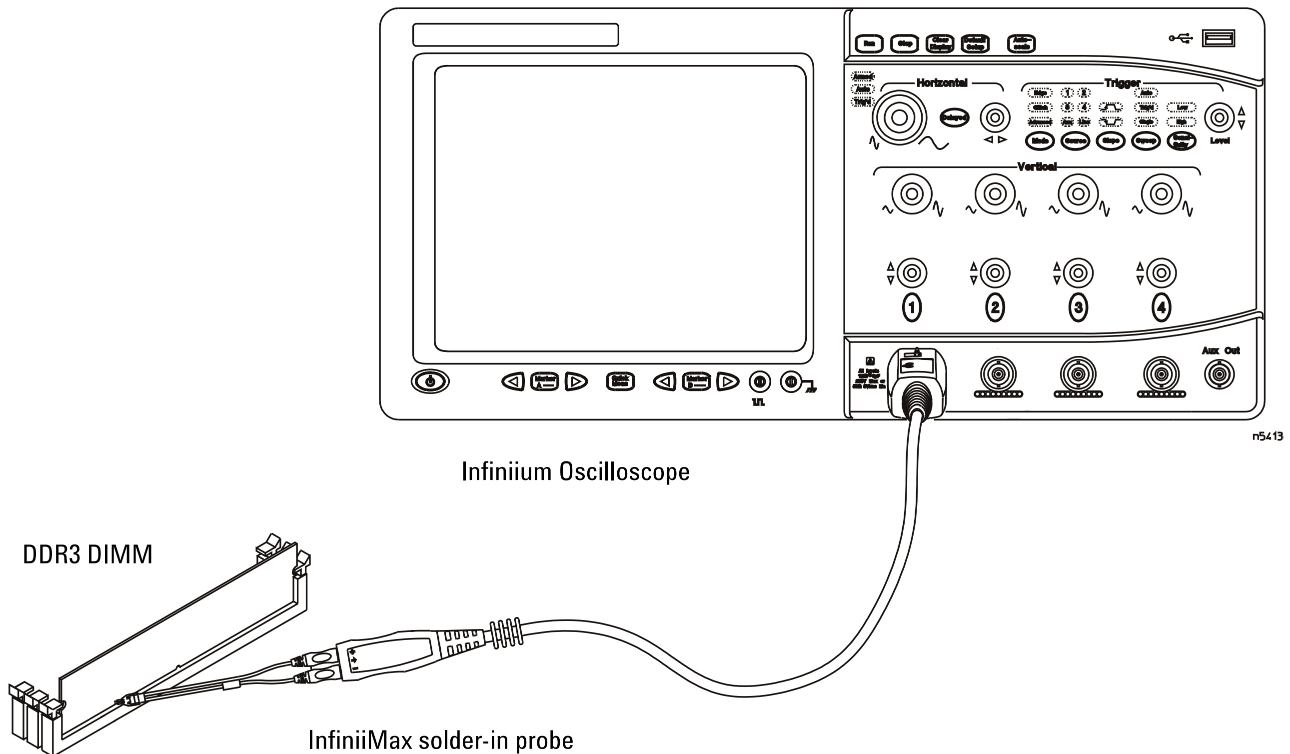


Figure 10 Probing for Single-Ended Signals Overshoot/Undershoot Tests

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channel shown in Figure 10 is just an example).

For more information on the probe amplifiers and differential probe heads, see Chapter 13, “InfiniiMax Probing,” starting on page 209.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the Set Up tab.

6 Select the Speed Grade options. For Single-Ended Signals Overshoot/Undershoot tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

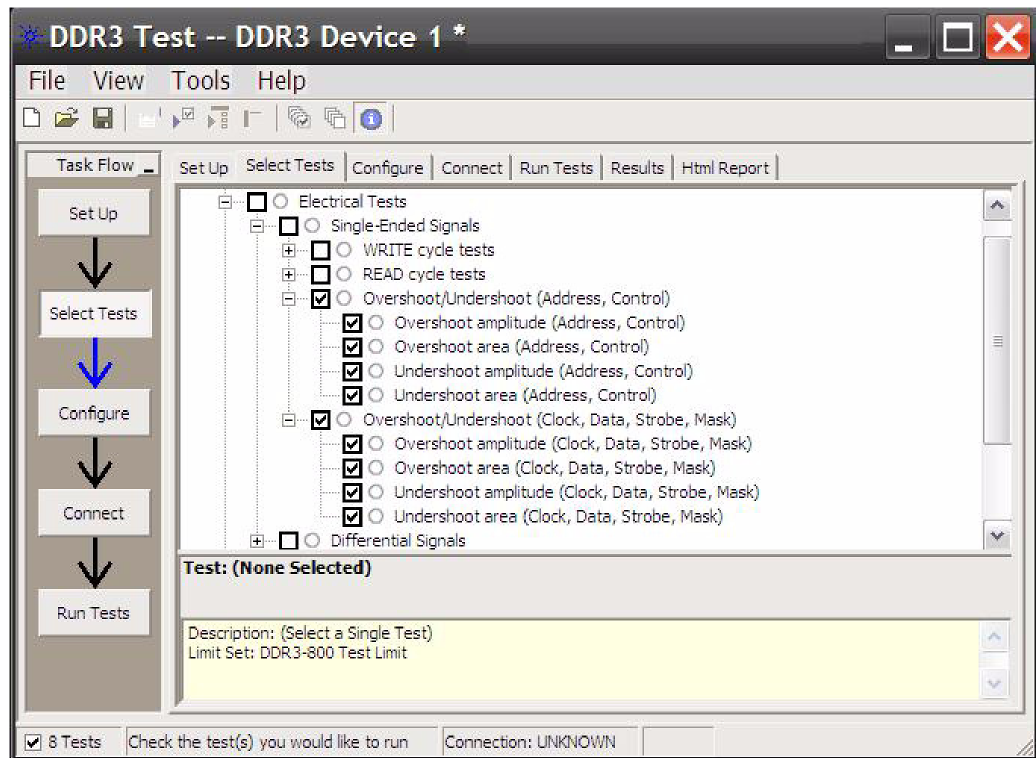


Figure 11 Selecting Single-Ended Signals Overshoot/Undershoot Tests

AC Overshoot Test Method of Implementation

The Overshoot test can be divided into two sub-tests: Overshoot amplitude and Overshoot area. The purpose of this test is to verify that the overshoot value of the test signal found from all regions of the acquired waveform is lower than or equal to the conformance limit of the maximum peak amplitude allowed for overshoot as specified in the JEDEC specification.

When there is an overshoot, the area is calculated based on the overshoot width and overshoot amplitude. The Overshoot area should be lower than or equal to the conformance limit of the maximum overshoot area allowed as specified in the JEDEC specification.

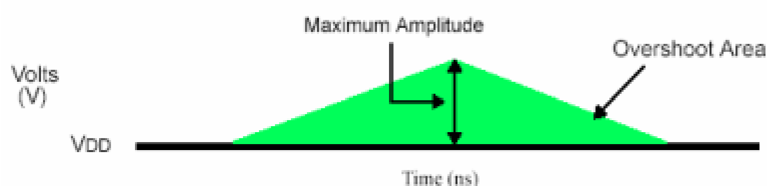


Figure 12 Address and Control Overshoot

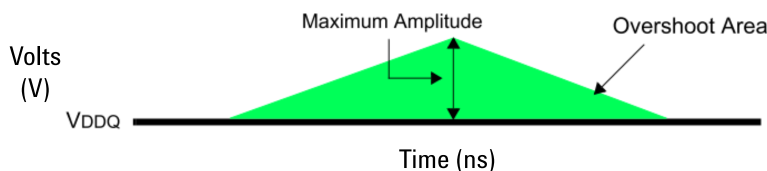


Figure 13 Clock, Data, Strobe, and Mask Overshoot

Signals of Interest

Based on the test definition (Read or Write):

- Data Signal OR
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals OR
- Clock Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 21 AC Overshoot Specification for Address and Control Pins

A0-A15, BA0-BA3, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, CKE, ODT

Parameter	**Specification**			
	DDR3-800	**DDR3-1066**	**DDR3-1333**	**DDR3-1600**
Maximum peak amplitude allowed for overshoot area	0.4 V	0.4 V	0.4 V	0.4 V
Maximum overshoot area above VDD	0.67 V-ns	0.5 V-ns	0.4 V-ns	0.33 V-ns

Table 22 AC Overshoot Specification for Clock, Data, Strobe and Mask Pins

CK, $\overline{\text{CK}}$, DQ, DQS, $\overline{\text{DQS}}$, DM

Parameter	**Specification**			
	DDR3-800	**DDR3-1066**	**DDR3-1333**	**DDR3-1600**
Maximum peak amplitude allowed for overshoot area	0.4 V	0.4 V	0.4 V	0.4 V
Maximum overshoot area above VDDQ	0.25 V-ns	0.19 V-ns	0.15 V-ns	0.13 V-ns

Test References

See Table 37 - AC Overshoot/Undershoot Specification for Address and Control Pins, and Table 38 - AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins, in the *JEDEC Standard JESD79- 3C*.

PASS Condition

The measured maximum voltage value should be less than or equal to the maximum overshoot value.

The calculated Overshoot area value should be less than or equal to the maximum Overshoot area allowed.

Measurement Algorithm

1. Set the number of sampling points to 2M samples.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Use TMAX and VMAX to get timestamp of maximum voltage on all regions of the acquired waveform.

4 Perform manual zoom waveform to maximum peak area.

5 Find the edges before and after the Overshoot Point at the Supply Reference Level in order to calculate the maximum overshoot length duration. Table below shows the supply reference level for each pin group:

Pin	Supply Reference Level
DDR3 Address and Control Pin	VDD
DDR3 Clock, Data, Strobe, and Mask Pin	VDDQ

6 Calculate Overshoot Amplitude. Overshoot Amplitude = VMAX - supply reference level (refer to table above)

7 Calculate the Overshoot area (V-ns)

   a Area of calculation is based on the area of calculation of a triangle where the Overshoot width is used as the triangle base and the Overshoot amplitude is used as the triangle height.

   b Area = 0.5 * base * height.

8 Compare test result to the compliance test limit.

AC Undershoot Test Method of Implementation

The Undershoot Test can be divided into two sub-tests: Undershoot amplitude and Undershoot area. The purpose of this test is to verify that the undershoot value of the test signal found from all regions of the acquired waveform is less than or equal to the conformance limit of the maximum peak amplitude allowed for undershoot as specified in the JEDEC specification.

When there is an undershoot, the area is calculated based on the undershoot width. The Undershoot area should be less than or equal to the conformance limit of the maximum undershoot area allowed as specified in the JEDEC specification.

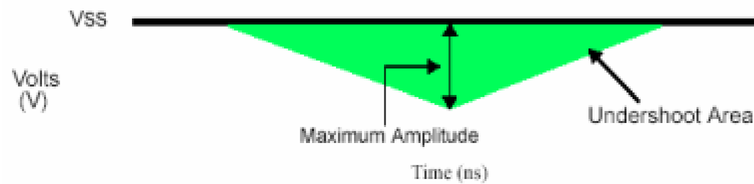


Figure 14 Address and Control Undershoot

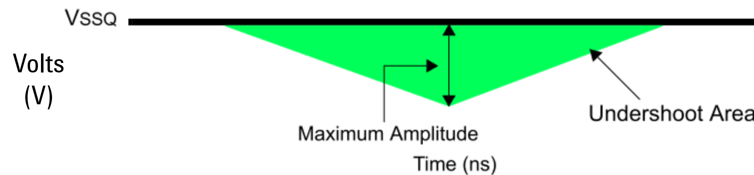


Figure 15 Clock, Data, Strobe, and Mask Undershoot

Signals of Interest

Based on the test definition (Read or Write):

- Data Signal OR
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals OR
- Clock Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 23 AC Overshoot/Undershoot Specification for Address and Control Pins

A0-A15, BA0-BA3, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT

Parameter	Specification			
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
Maximum peak amplitude allowed for undershoot area	0.4 V	0.4 V	0.4 V	0.4 V
Maximum undershoot area below VSS	0.67 V-ns	0.5 V-ns	0.4 V-ns	0.33 V-ns

Table 24 AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins

CK, $\overline{CK}$, DQ, DQS, $\overline{DQS}$, DM

Parameter	Specification			
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
Maximum peak amplitude allowed for undershoot area	0.4 V	0.4 V	0.4 V	0.4 V
Maximum undershoot area below VSSQ	0.25 V-ns	0.19 V-ns	0.15 V-ns	0.13 V-ns

Test References

See Table 37 - AC Overshoot/Undershoot Specification for Address and Control Pins, and Table 38 - AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins, in the *JEDEC Standard JESD79- 3C*.

PASS Condition

The measured minimum voltage value for the test signal should be less than or equal to the maximum undershoot value.

The calculated undershoot area value should be less than or equal to the maximum undershoot area allowed.

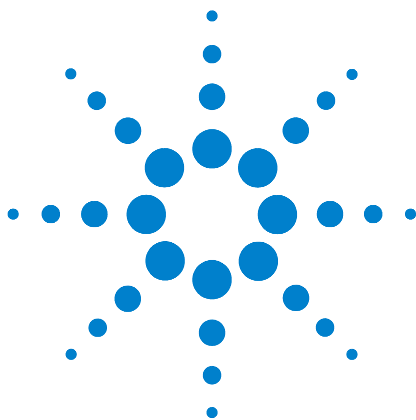
Measurement Algorithm

1. Set the number of sampling points to 2M samples.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

3 Use TMIN and VMIN to get timestamp of minimum voltage on all regions of the acquired waveform.
4 Perform manual zoom waveform to minimum peak area.
5 Find the edges before and after the Undershoot Point at the GND (-0V) level in order to calculate the maximum undershoot length duration. Table below shows the supply reference level for each pin group:

Pin	Supply Reference Level
DDR3 Address and Control Pin	VSS
DDR3 Clock, Data, Strobe, and Mask Pin	VSSQ

6 Calculate Undershoot Amplitude. Undershoot Amplitude = 0 - VMIN.
7 Calculate the Undershoot area (V-ns)
   a Area of calculation is based on the area of calculation of a triangle where the Undershoot width is used as the triangle base and the Undershoot amplitude is used as the triangle height.
   b Area = 0.5 * base * height.
8 Compare test result to the compliance test limit.



6 Differential Signals AC Input Parameters Tests

Probing for Differential Signals AC Input Parameters Tests 80
VIX(AC), AC Differential Input Cross Point Voltage -Test Method of Implementation 83

This section provides the Methods of Implementation (MOIs) for Differential Signals AC Input tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Differential Signals AC Input Parameters Tests

When performing the Differential Signals AC Input Parameters tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for the Differential Signals AC Input Parameters tests may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance application for the exact number of probe connections.

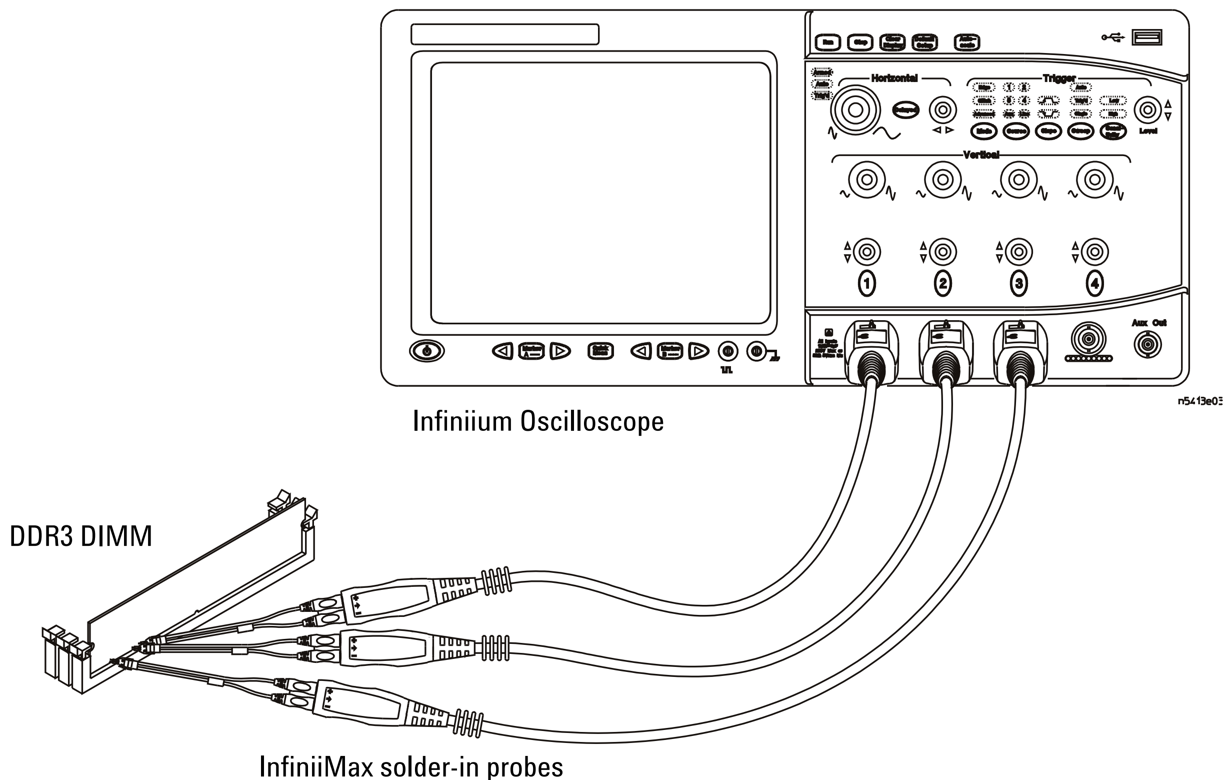


Figure 16 Probing for Differential Signals AC Input Parameters Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 16 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 13, “InfiniiMax Probing,” starting on page 209.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.
2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.
3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.
4 Connect the oscilloscope probes to any channels of the oscilloscope.
5 In the DDR3 Test application, click the Set Up tab.
6 Select the Speed Grade options. For Differential Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.
7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

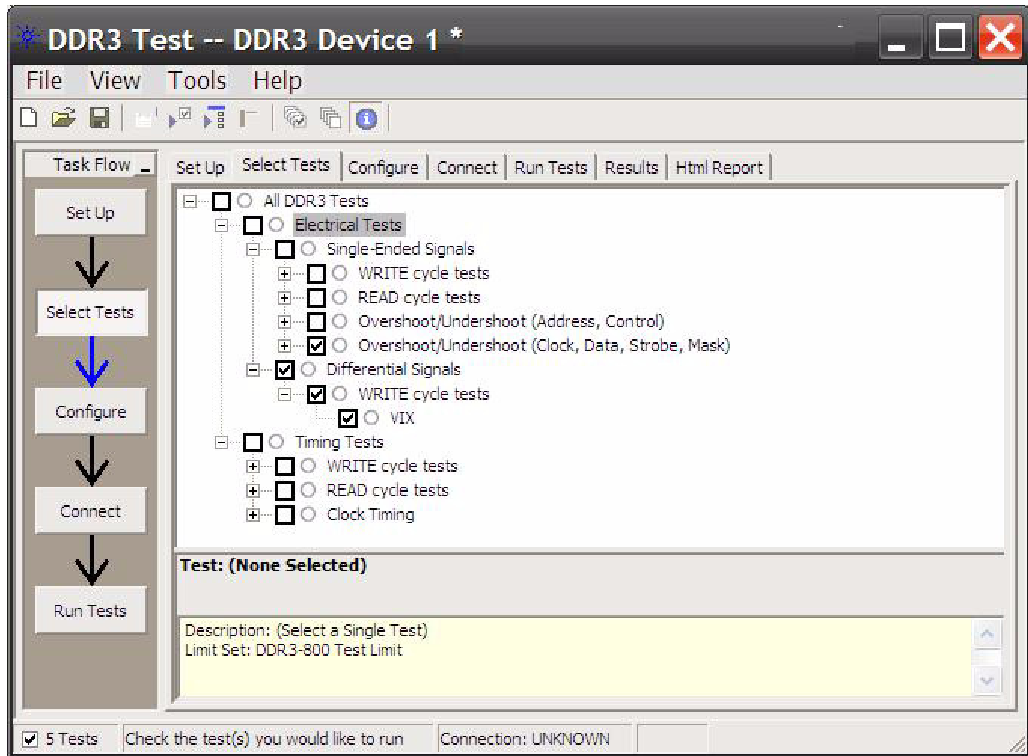


Figure 17 Selecting Differential Signals AC Input Parameters Tests

$V_{IX(AC)}$, AC Differential Input Cross Point Voltage -Test Method of Implementation

The purpose of this test is to verify the crossing point of the input differential test signals pair is within the conformance limits of the $V_{IX(AC)}$ as specified in the JEDEC specification.

The value of V_{DDQ} which directly affects the conformance upper limit is defaulted to 1.50V. However, users have the flexibility to change this value.

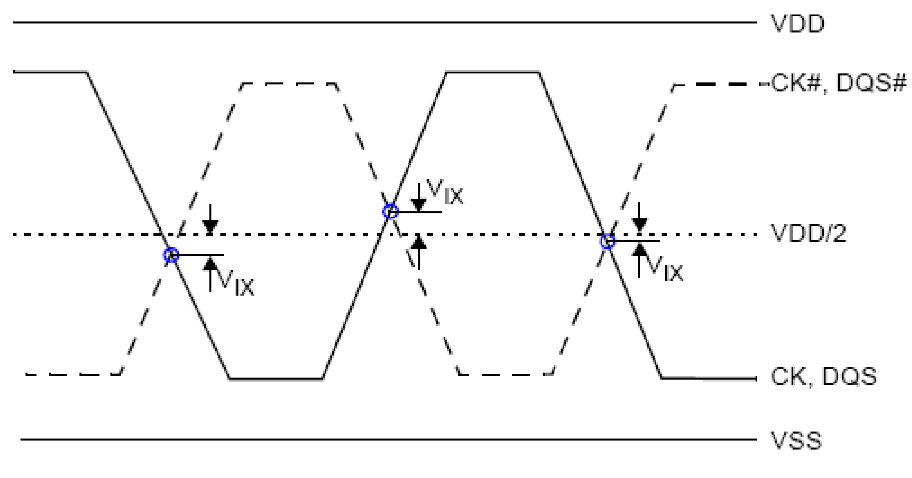


Figure 18 V_{IX} AC Differential Input Voltage

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (supported by Data Signals) OR
- Clock Signals

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)
- Supporting Pin (only required when PUT is DQS)

Test Definition Notes from the Specification

Table 25 Cross Point Voltage for Differential Input Signals (CK, DQS)

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Units	Notes
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2 for CK, CK#	-150	150	mV	
		-175	175	mV	1
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS#	-150	150	mV	
NOTE 1. Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL/VSEH of at least VDD/2 ±250mV, and when the differential slew rate of CK - CK# is larger than 3V/ns. Refer to VSEL and VSEH standard values.					

Test References

See Table 29 - Cross Point Voltage for Differential Input Signals (CK, DQS), in the *JEDEC Standard JESD79- 3C*.

PASS Condition

The measured crossing point value for the differential test signals pair should be within the conformance limits of $V_{IX(AC)}$ value.

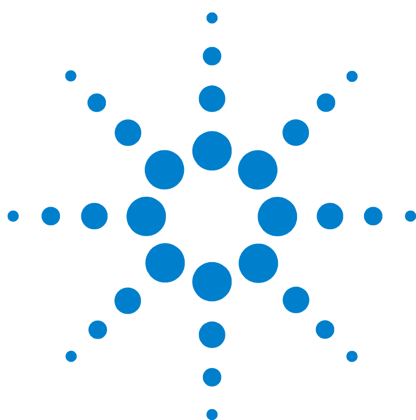
Measurement Algorithm

For PUT is DQS and DQS#:

1 Obtain sample or acquire data waveforms.
2 Use Subtract function to generate the differential waveform from two source input.
3 Split read and write burst of the acquired signal.
4 Take the first valid WRITE burst found.
5 Find all differential DQS crossing that cross 0V.
6 Use VTIME to get the actual crossing point voltage value using the timestamp obtained.
7 Determine the worst result from the set of $V_{IX\ (AC)}$ measured.

For PUT is CLK and CLK#:

1. Obtain sample or acquire data waveforms.
2. Use Subtract function to generate the differential waveform from two source input.
3. Find the first 10 differential CLK crossing that cross 0V.
4. Use VTIME to get the actual crossing point voltage value using the timestamp obtained.
5. Determine the worst result from the set of $V_{IX\ (AC)}$ measured.



7
Clock Timing (CT) Tests

Probing for Clock Timing Tests 88
Clock Period Jitter - tJIT(per) - Test Method of Implementation 90
Cycle to Cycle Period Jitter - tJIT(cc) - Test Method of Implementation 92
Cumulative Error - tERR(nper) - Test Method of Implementation 94
Average High Pulse Width - tCH(avg) - Test Method of Implementation 97
Average Low Pulse Width - tCL(avg) - Test Method of Implementation 99
Half Period Jitter - tJIT(duty) - Test Method of Implementation 101
Average Clock Period - tCK(avg) - Test Method of Implementation 103

This section provides the Methods of Implementation (MOIs) for Clock Timing tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

NOTE

Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Clock Timing Tests

When performing the Clock Timing tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for Clock Timing tests may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

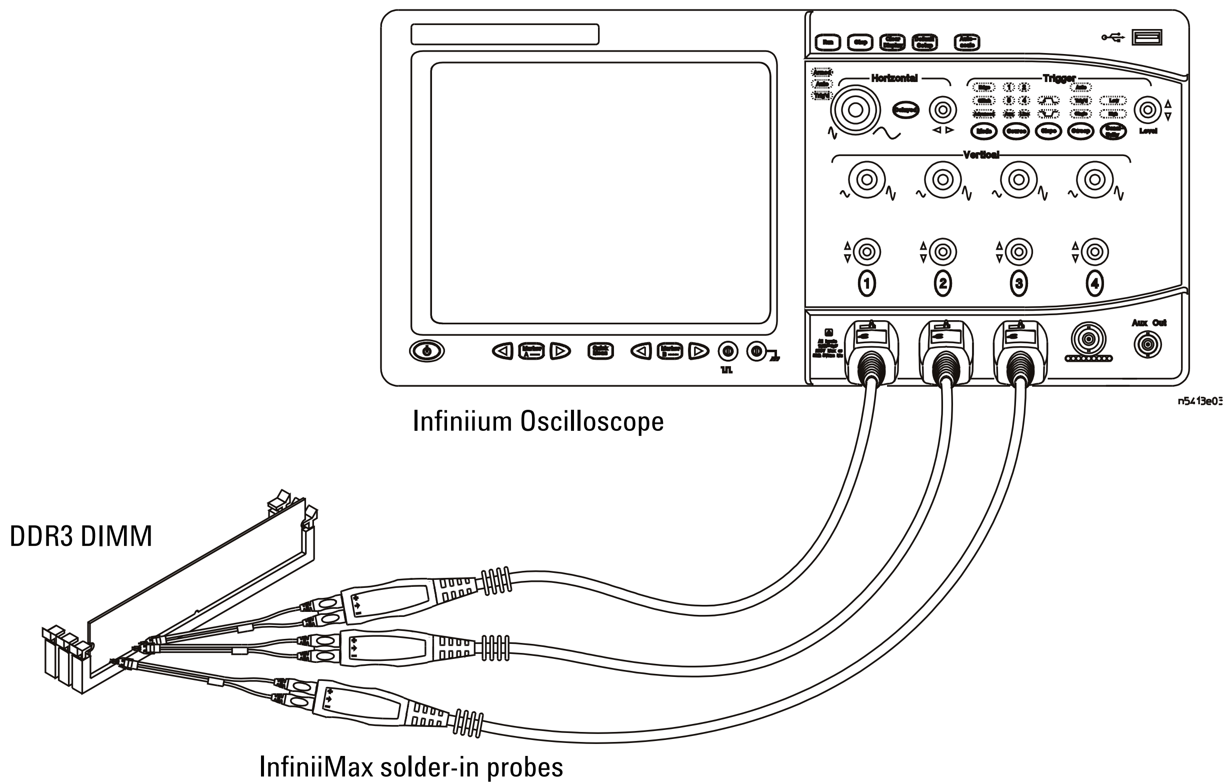


Figure 19 Probing for Clock Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 19 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 13, “InfiniiMax Probing,” starting on page 209.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the Set Up tab.

6 Select the Speed Grade options. For Clock Timing Tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

Clock Period Jitter - tJIT(per) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock.

Signals of Interest

Based on the test definition (Read or Write):

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 26 Clock Period Jitter Test

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Clock Period Jitter	tJIT(per)	-100	100	-90	90	ps	

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Clock Period Jitter	tJIT(per)	-80	80	-70	70	ps	

Pass Condition

The tJIT(per) measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. This measurement measures the difference between every period inside a 200 cycle window with the average of the whole window.
2. First, calculate the average for periods 1-200.
3. Measure the difference between period #1 and the average. Save the result as a measurement result.

4 Measure the difference between period #2 and the average. Save the answer.
5 Continue this same procedure until period #200 is compared to the average (200 measurements are generated).
6 Slide the window by one and measure the average of 2-201.
7 Compare period #2 with the new average. Continue the comparison for period #3, #4, ... #200, #201 (200 more measurements are generated, 400 total now).
8 Next, slide the window by one and measure the average of periods 3-202.
9 Compare period #3 with the new average. Continue the comparison for period #4, #5, ... #201, #202 (200 more measurements so now the total is 600 measurements).
10 Check these 600 measurements for the smallest and largest values (worst case values).
11 Compare test result to compliance test limit.

Test References

See Table 65-Timing Parameters by Speed Bin in the *JEDEC Standard JESD79-3C*.

Cycle to Cycle Period Jitter - tJIT(cc) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement. The purpose of this test is to measure the difference in the clock period between two consecutive clock cycles. The tJIT(cc) Rising Edge Measurement measures the clock period from the rising edge of a clock cycle to the next rising edge.

Signals of Interest

Based on the test definition (Read or Write):

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 27 Cycle to Cycle Period Jitter Test

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Cycle to Cycle Period Jitter	tJIT(cc)	200		180		ps	

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Cycle to Cycle Period Jitter	tJIT(cc)	160		140		ps	

Pass Condition

The tJIT(cc) measurement value should be within the conformance limits as specified in the JEDEC specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the difference between every adjacent pair of periods.
2. Generate 201 measurement results.
3. Check the results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

Test References

See Table 65-Timing Parameters by Speed Bin in the *JEDEC Standard JESD79- 3C*.

Cumulative Error - tERR(nper) - Test Method of Implementation

This Cumulative Error (across “n” cycles) test is applicable to the Rising Edge Measurement. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock. Supported measurements include multiple cycle windows with values of “n” (for “n” cycles) where n > 5 but less than 50.

Signals of Interest

Based on the test definition (Read or Write):

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 28 Cumulative Error Across n Cycles

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		min	max	min	max	min	max	min	max	
Cumulative error across 2 cycles	tERR(2per)	-147	147	-132	132	-118	118	-103	103	ps
Cumulative error across 3 cycles	tERR(3per)	-175	175	-157	157	-140	140	-122	122	ps
Cumulative error across 4 cycles	tERR(4per)	-194	194	-175	175	-155	155	-136	136	ps
Cumulative error across 5 cycles	tERR(5per)	-209	209	-188	188	-168	168	-147	147	ps
Cumulative error across 6 cycles	tERR(6per)	-222	222	-200	200	-177	177	-155	155	ps
Cumulative error across 7 cycles	tERR(7per)	-232	232	-209	209	-186	186	-163	163	ps
Cumulative error across 8 cycles	tERR(8per)	-241	241	-217	217	-193	193	-169	169	ps
Cumulative error across 9 cycles	tERR(9per)	-249	249	-224	224	-200	200	-175	175	ps
Cumulative error across 10 cycles	tERR(10)	-257	257	-231	231	-205	205	-180	180	ps
Cumulative error across 11 cycles	tERR(11)	-263	263	-237	237	-210	210	-184	184	ps
Cumulative error across 12 cycles	tERR(12)	-269	269	-242	242	-215	215	-188	188	ps
Cumulative error across 13, 14, ... 49, 50 cycles	tERR(11-50)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 + 0.68ln(n))*tJIT(per)max								ps

Pass Condition

The tERR measurement value should be within the conformance limits as specified in the JEDEC Specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. tERR(2per) is similar to tJIT(per), except it makes a small 2-cycle window inside the big 200 cycle window and compares the average of the small window with the average of the big window.
2. First, calculate the average for periods 1-200.
3. Calculate the average of periods 1-2.
4. Measure the difference between these two averages and save this as a measurement result.
5. Calculate the average of period 2-3 and measure the difference between this average and the big window average.

6 Continue this same procedure until it compares the average of periods 199-200 to the big window average (so far, 199 measurement result generated).
7 Next, slide the big window by one and repeat, starting by comparing the average of periods 2-3 with the new big window average until it finishes by comparing periods 200-201 with the big window (by now 199 more measurements have been taken for a total of 398 measurements so far).
8 Slide the big window by one again and repeat the same procedure (making a total of 597 measurement values).
9 Check the 597 results for the smallest and largest values (worst case values).
10 Compare the test result to the compliance limit.
11 tERR(3per) is the same as tERR(2per) except the small window size is 3 periods wide. tERR(4per) uses small window size of 4 periods, and tERR(5per) uses 5 periods.
12 tERR(6-10per) executes tERR(6per), tERR(7per), tERR(8per), tERR(9per) and tERR(10per), combines all the measurement results together into one big pool and checks for the smallest and largest value.
13 tERR(11-50per) does the same for tERR(11per) through tERR(50per).

Test References

See Table 65-Timing Parameters by Speed Bin in the *JEDEC Standard JESD79-3C*.

Average High Pulse Width - tCH(avg) - Test Method of Implementation

The purpose of this test is to measure the average duty cycle of all the positive pulse widths within a window of 200 consecutive cycles.

Signals of Interest

Based on the test definition (Read or Write):

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 29 Average High Pulse Width Test

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Average High Pulse Width	tCH(avg)	0.47	0.53	0.47	0.53	tCK(avg)	

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Average High Pulse Width	tCH(avg)	0.47	0.53	0.47	0.53	tCK(avg)	

Pass Condition

The tCH measurement value should be within the conformance limits as specified in the JEDEC Specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding “window” of 200 cycles.
2. Measure the width of the high pulses 1-200 and determine the average value for this window. (generated 1 measurement result).
3. Measure the width of the high pulses 2-201 and determine the average value for this window. (by now, generate a total of 2 measurement results).

4 Measure the width of the high pulses 3-202 and determine the average value for this window. (by now, generate a total of 3 measurement results).
5 Check the total 3 results for the smallest and largest values (worst case values).
6 Compare the test results against the compliance test limits.

Test References

See Table 65-Timing Parameters by Speed Bin in the *JEDEC Standard JESD79-3C*.

Average Low Pulse Width - tCL(avg) - Test Method of Implementation

The purpose of this test is to measure the average duty cycle of all the negative pulse widths within a window of 200 consecutive cycles.

Signals of Interest

Based on the test definition (Read or Write):

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 30 Average Low Pulse Width Test

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Average Low Pulse Width	tCL(avg)	0.47	0.53	0.47	0.53	tCK(avg)	

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Average Low Pulse Width	tCL(avg)	0.47	0.53	0.47	0.53	tCK(avg)	

Pass Condition

The tCL measurement value should be within the conformance limits as specified in the JEDEC Specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding "window" of 200 cycles.
2. Measure the width of the low pulses 1-200 and determine the average value for this window. (generated 1 measurement result).
3. Measure the width of the low pulses 2-201 and determine the average value for this window. (by now, generate a total of 2 measurement results).

4 Measure the width of the low pulses 3-202 and determine the average value for this window. (by now, generate a total of 3 measurement results).
5 Check the total 3 results for the smallest and largest values (worst case values).
6 Compare results against the compliance test limits.

Test References

See Table 65-Timing Parameters by Speed Bin in the *JEDEC Standard JESD79-3C*.

Half Period Jitter - tJIT(duty) - Test Method of Implementation

The Half Period Jitter tJIT(duty) can be divided into tJIT(CH) Jitter Average High and tJIT(LH) Jitter Average Low. The tJIT(CH) Jitter Average High Measurement measures between a positive pulse width of a cycle in the waveform, and the average positive pulse width of all cycles in a 200 consecutive cycle window. tJIT(LH) Jitter Average Low Measurement measures between a negative pulse width of a cycle in the waveform and the average negative pulse width of all cycles in a 200 consecutive cycle window.

Signals of Interest

Based on the test definition (Read or Write):

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 31 Duty Cycle Jitter Test

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	ps	

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	ps	

NOTE: Due to the unavailability of limit values for this test parameter in the specification document, the limit for this test is left open by setting the minimum and maximum to very large values (min = -99E36, max = 99E36)

Pass Condition

The tJIT(duty) measurement value should be within the conformance limits as specified in the JEDEC Specification.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

tJIT(CH):

1 This measurement measures the difference between every high pulse width inside a 200 cycle window with the average of the whole window.
2 First calculate the average for high pulse width 1-200.
3 Measure the difference between high pulse width #1 and the average. Save the answer as a measurement result.
4 Measure the difference between high pulse width #2 and the average. Save the answer as a measurement result.
5 Continue this same procedure until high pulse #200 is compared to the average (200 measurements).
6 Slide the window by one and measure the average of 2-201.
7 Compare high pulse #2 with the new average. Continue the comparisons for high pulse width #3, #4, ... #200, #201 (200 more measurements so 400 total so far).
8 Slide the window by one and measure the average of 3-202.
9 Compare high pulse width #3 with the new average. Continue the comparisons for high pulse width #4, #5, ... #201, #202 (200 more measurements so 600 total measurements).
10 Check these 600 results for the smallest and largest values (worst case values).
11 Compare the test results against the compliance test limits.

tJIT(LH):

1 This measurement is similar to tJIT(CH) above except, instead of using high pulse widths, it uses low pulse widths for testing comparison.

Test References

See Table 65-Timing Parameters by Speed Bin in the *JEDEC Standard JESD79-3C*.

Average Clock Period - tCK(avg) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement. tCK(avg) is average clock period within 200 consecutive cycle window. The tCK(avg) Rising Edge Measurement measures the period from the rising edge of a cycle to the next rising edge within the waveform window.

Signals of Interest

Based on the test definition (Read or Write):

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is any of the signals of interest defined above)

Test Definition Notes from the Specification

Table 32 DDR3-800 Speed Bins and Operating Conditions

Speed Bin			DDR3-800D		DDR3-800E		Units	Specific Notes
CL - nRCD - nRP			5-5-5		6-6-6			
Parameter		Symbol	Min	Max	Min	Max		
CL = 6	CWL = 5	tCK(avg)	2.5	3.3	2.5	3.3	ns	1,2,3

Table 33 DDR3-1066 Speed Bins and Operating Conditions

Speed Bin			DDR3-1066E		DDR3-1066F		DDR3-1066G		Units	Specific Notes
CL - nRCD - nRP			6-6-6		7-7-7		8-8-8			
Parameter		Symbol	Min	Max	Min	Max	Min	Max		
CL = 8	CWL = 6	tCK(avg)	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3

Table 34 DDR3-1333 Speed Bins and Operating Conditions

Speed Bin			DDR3-1333F (optional)		DDR3-1333G		DDR3-1333H		DDR3-1333J (optional)		Units	Specific Notes
CL - nRCD - nRP			7-7-7		8-8-8		9-9-9		10-10-10			
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
CL = 10	CWL = 7	tCK(avg)	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	1.5	< 1.875	ns	1,2,3
			(optional)		(optional)		(optional)				ns	5

Table 35 DDR3-1600 Speed Bins and Operating Conditions

Speed Bin			DDR3-1600G (optional)		DDR3-1600H		DDR3-1600J		DDR3-1600K (optional)		Units	Specific Notes
CL - nRCD - nRP			8-8-8		9-9-9		10-10-10		11-11-11			
Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
CL = 8	CWL = 6	tCK(avg)	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	ns	1,2,3
			(optional)		(optional)		(optional)				ns	5

Pass Condition

The tCK(avg) measurement value should be within the conformance limits as specified in the JEDEC Specification.

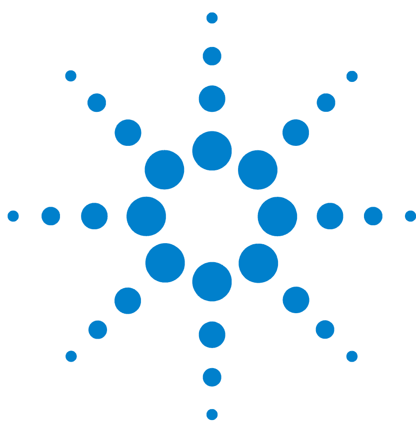
Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1 This measurement measures a sliding “window” of 200 cycles.
2 First, calculate the average period value for periods 1-200.
3 Calculate the average period value for periods 2-201.
4 Calculate the average period value for periods 3-202 (by now, 3 measurement results are generated).
5 Check the results for the smallest and largest values (worst case values).
6 Compare the test results against the compliance test limits.

Test References

See Table 61-64 in the *JEDEC Standard JESD79-3C*.



8
Data Strobe Timing (DST) Tests

Probing for Data Strobe Timing Tests 108
tDQSCK, DQS Output Access Time from CK/CK #- Test Method of Implementation 110
tLZ(DQS), DQS Low-Impedance Time from CK/CK# - Test Method of Implementation 112
tDQSS, DQS Latching Transition to Associated Clock Edge - Test Method of Implementation 114
tDQSH, DQS Input High Pulse Width - Test Method of Implementation 116
tDQSL, DQS Input Low Pulse Width - Test Method of Implementation 118
tDSS, DQS Falling Edge to CK Setup Time - Test Method of Implementation 120
tDSH, DQS Falling Edge Hold Time from CK - Test Method of Implementation 123
tWPST, Write Postamble - Test Method of Implementation 125
tWPRE, Write Preamble - Test Method of Implementation 127
tRPRE, Read Preamble - Test Method of Implementation 129
tRPST, Read Postamble - Test Method of Implementation 131

This section provides the Methods of Implementation (MOIs) for Data Strobe Timing tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

NOTE

Both XYZ# and $\overline{XYZ}$ are referring to compliment. Thus, CK# is the same as $\overline{CK}$.

Probing for Data Strobe Timing Tests

When performing the Data Strobe Timing tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for Data Strobe Timing tests may look similar to the following diagram. Refer to the Connection tab in DDR3 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

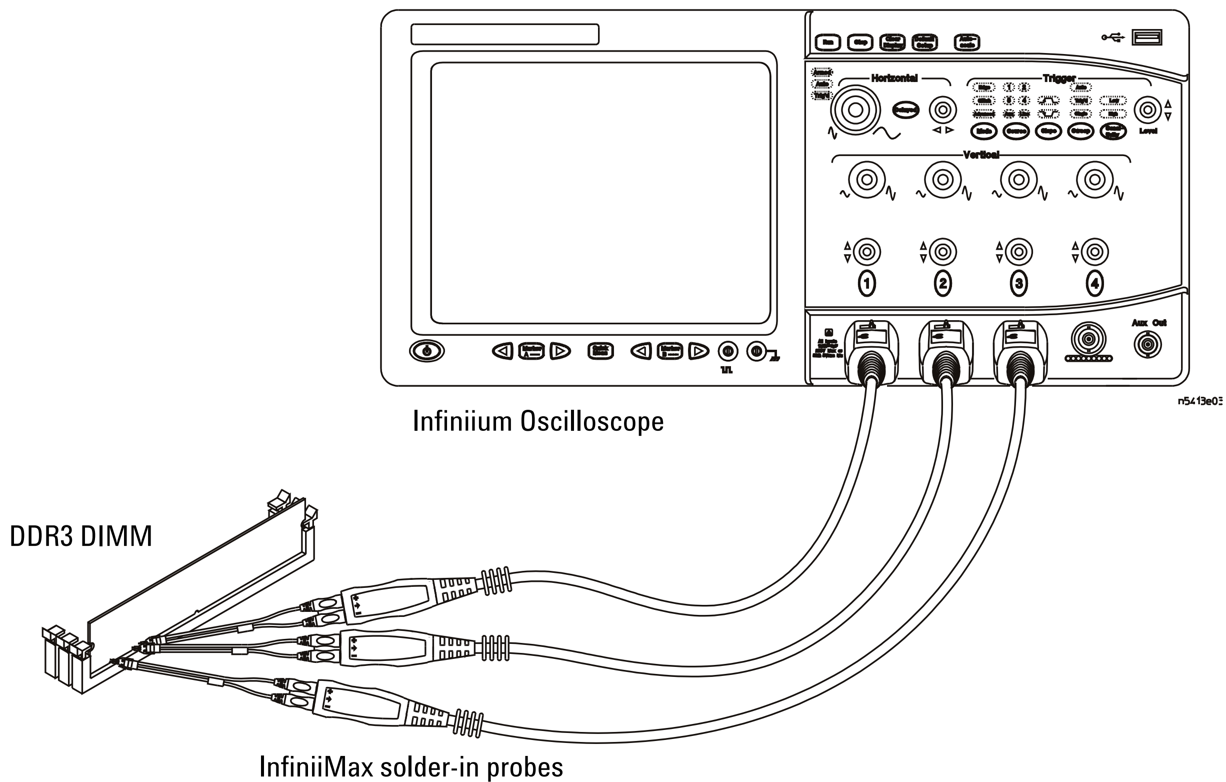


Figure 20 Probing for Data Strobe Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 20 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 13, "InfiniiMax Probing," starting on page 209.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the Set Up tab.

6 Select the Speed Grade options. For Clock Timing Tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

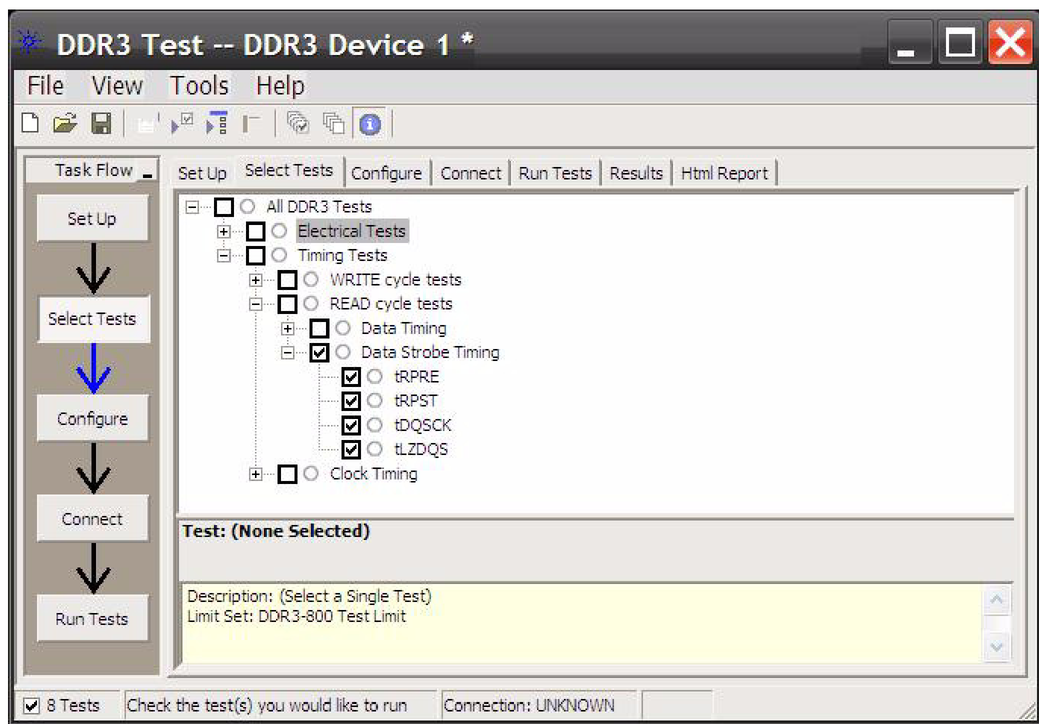


Figure 21 Selecting Data Strobe Timing Tests

tDQSCK, DQS Output Access Time from CK/CK #- Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS rising edge) access time to the nearest rising or falling edge of the clock is within the conformance limit as specified in the JEDEC specification.

There is tDQSCK(min) and tDQSCK(max) as shown in Figure 22. From the specification, you can observe that the minimum value is at negative while the maximum is at positive.

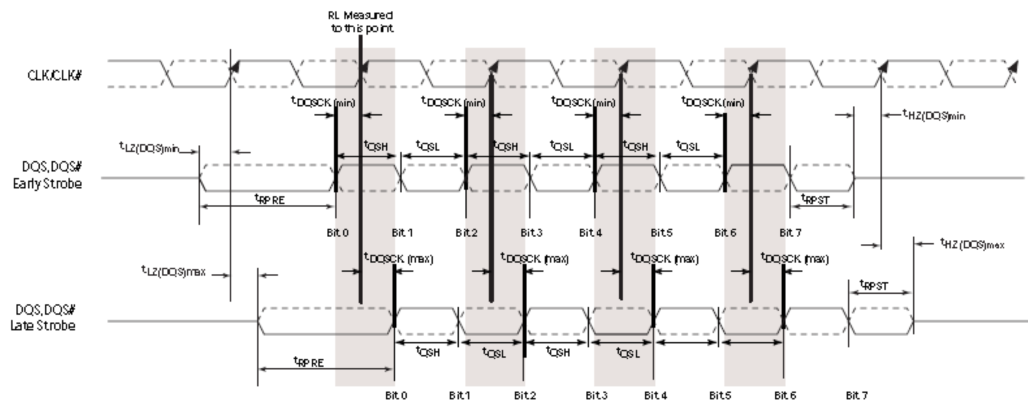


Figure 22 DQS Output Access Time from CK/CK#

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 36 DQS Output Access Time Test

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# rising edge output access time from CK/CK#	tDQSCK	-400	400	-300	300	ps	13, f

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# rising edge output access time from CK/CK#	tDQSCK	-255	255	-225	225	ps	13, f

NOTE 12: Please refer to page 161, *JEDEC Standard JESD79- 3*.

NOTE 13: Please refer to page 172, *JEDEC Standard JESD79- 3*.

PASS Condition

The measured time interval between the data strobe access output and the rising edge of the clock should be within the specification limit.

Measurement Algorithm

1 Acquire and split Read and Write burst of the acquired signal.
2 Take the first valid Read burst found.
3 Find all valid rising DQS crossings at V_{REF} in the said burst.
4 For all DQS crossings found, locate the nearest rising Clock crossing at 0V.
5 Take the time difference from DQS crossing to the corresponding Clock crossing as the tDQSCK.
6 Determine the worst result from the set of tDQSCK measured.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.

tLZ(DQS), DQS Low-Impedance Time from CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS starts driving (from tristate to high/low state) to the clock signal crossing, is within the conformance limit as specified in the JEDEC Specification.

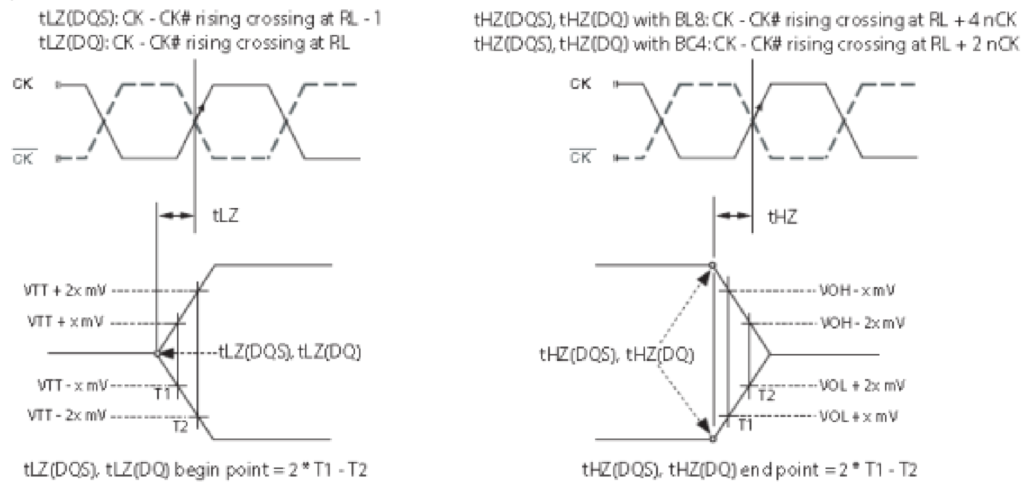


Figure 23 DQS Low-Impedance Time From CK/CK#

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (supported by Data Signals)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 37 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS and DQS# low impedance time	tLZ(DQS)	-800	400	-600	300	ps	13, 14, f

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS and DQS# low impedance time	tLZ(DQS)	-500	250	-450	225	ps	13, 14, f

NOTE 12,13,14: Please refer to page 160, *JEDEC Standard JESD79- 3*.

PASS Condition

The measured time interval from the point where the DQS starts to transit from tristate to the moment when it starts to drive high/low (high impedance state to high/low state) to the clock signal crossing point, should be within the specification limit.

Measurement Algorithm

1. Acquire and split the Read and Write burst of the acquired signal.
2. Take the first valid READ burst found.
3. Find tLZBeginPoint of the said burst.
4. Find the nearest Clock rising edge.
5. tLZ(DQS) is the time interval of the found Clock rising edge's crossing point to the tLZBeginPoint found.
6. Report tLZ(DQS)

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.

tDQSS, DQS Latching Transition to Associated Clock Edge - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS falling edge) access time to the associated clock (crossing point) is within the conformance limit as specified in the JEDEC Specification.

Figure 24 DQS Latching Transition to Associated Clock Edge

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)

- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 38 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# rising edge to CHK/CK# rising edge	tDQSS	-0.25	0.25	-0.25	0.25	tCK(avg)	c

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# rising edge to CHK/CK# rising edge	tDQSS	-0.25	0.25	-0.27	0.27	tCK(avg)	c

NOTE c: Please refer to page 160, *JEDEC Standard JESD79- 3*.

PASS Condition

The measured time interval between the rising edge of the data strobe access output and the clock crossing should be within specification limit.

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising DQS crossings in the said burst.
4. For all DQS crossings found, locate the nearest Clock rising crossing.
5. Take the time difference from DQS crossing to Clock crossing as the tDQSS.
6. Determine the worst result from the set of tDQSS measured.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.

tDQSH, DQS Input High Pulse Width - Test Method of Implementation

The purpose of this test is to verify that the width of the high level of the data strobe signal is within the conformance limit as specified in the JEDEC Specification.

Figure 25 DQS Input High Pulse Width

Signals of Interest

Based on the test definition (WRITE cycle only):

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 39 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	tCK(avg)	30, 31

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	tCK(avg)	30, 31

PASS Condition

The measured pwidth of the data strobe signal should be within specification limit.

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising and falling DQS crossings in the said burst.
4. tDQSH is the time starting from a rising edge of the DQS and ending at the following falling edge.
5. Collect all tDQSH.
6. Determine the worst result from the set of tDQSH measured.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.

tDQSL, DQS Input Low Pulse Width - Test Method of Implementation

The purpose of this test is to verify that the width of the low level of the clock signal is within the conformance limit as specified in the JEDEC Specification.

Figure 26 DQS Input Low Pulse Width

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 40 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	tCK(avg)	29,31

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	tCK(avg)	29,31

PASS Condition

The measured nwidth of the clock signal should be within specification limit.

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising and falling DQS crossings in the said burst.
4. tDQSL is the time starting from a falling edge of the DQS and ending at the following rising edge.
5. Collect all tDQSL.
6. Determine the worst result from the set of tDQSL measured.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.

tDSS, DQS Falling Edge to CK Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the falling edge of the data strobe (DQS falling edge) output access time to the clock setup time, is within the conformance limit as specified in the JEDEC Specification.

Figure 27 DQS Falling Edge to CK Setup Time

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 41 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	0.2	-	tCK(avg)	c, 32

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	0.18	-	tCK(avg)	c, 32

NOTE c: Please refer to page 160, *JEDEC Standard JESD79- 3*.

PASS Condition

The measured time interval between the falling edge of the data strobe access output to the associated clock setup time should be within the specification limit.

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid falling DQS crossings in the said burst.
4. For all falling DQS crossings found, locate all nearest next rising Clock edges.
5. tDSS is the time between falling DQS crossings and the Clock rising edges found.
6. Collect all tDSS.
7. Determine the worst result from the set of tDSS measured.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.

tDSH, DQS Falling Edge Hold Time from CK - Test Method of Implementation

The purpose of this test is to verify that the time interval from the falling edge of the data strobe output access time to the hold time of the clock, must be within the conformance limit as specified in the JEDEC Specification.

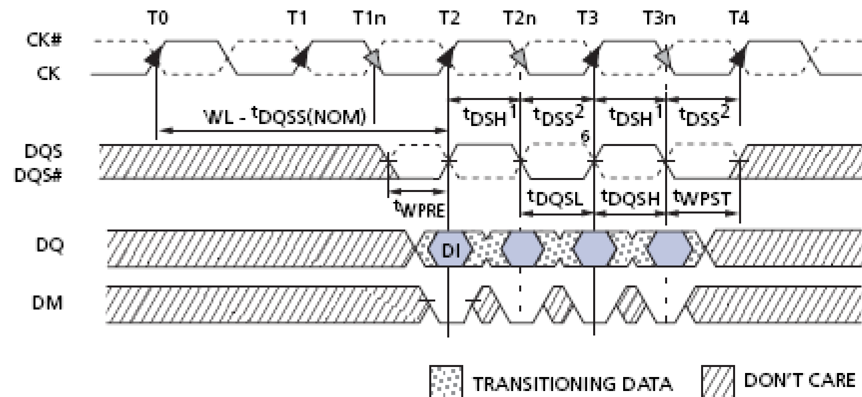


Figure 28 DQS Falling Edge Hold Time

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (supported by Data Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 42 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	0.2	-	tCK(avg)	c, 32

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	0.18	-	tCK(avg)	c, 32

NOTE c: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval between the falling edge of the data strobe hold time from the associated clock crossing edge should be within the specification limit.

Measurement Algorithm

1 Acquire and split the Read and Write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid falling DQS crossings in the said burst.
4 For all falling DQS crossings found, locate all nearest prior rising Clock edges.
5 tDSH is the time between falling DQS crossings and the Clock rising edges' crossing point found.
6 Collect all tDSH.
7 Determine the worst result from the set of tDSH measured.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3C*.

tWPST, Write Postamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS is no longer driving (from high/low state to high impedance) from the last DQS signal crossing (last bit of the write data burst) for the Write cycle, is within the conformance limit as specified in the JEDEC Specification.

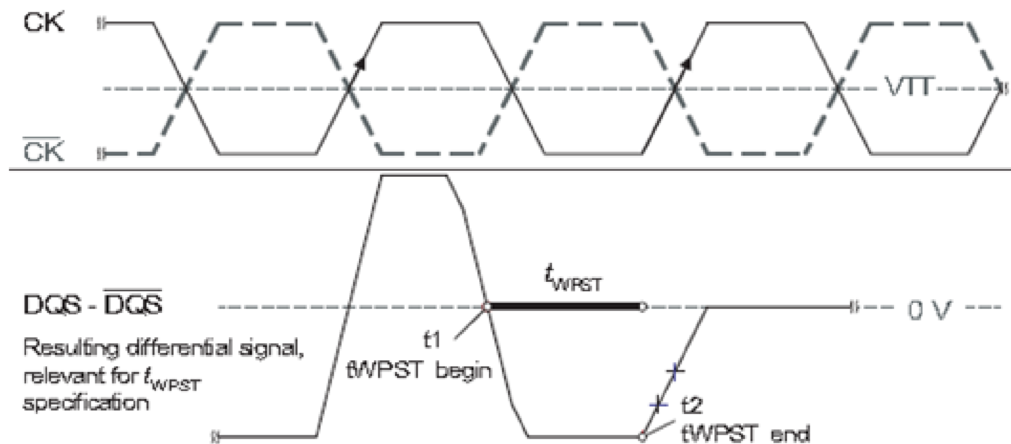


Figure 29 tWPST Transitions and Endpoints Calculation

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 43 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	0.3	-	tCK(avg)	

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	0.3	-	tCK(avg)	

NOTE 1: Please refer to page 160, *JEDEC Standard JESD79- 3*.

PASS Condition

The measured time interval between the last DQS signal crossing point and the point where the DQS starts to transit from high/low state to high impedance should be within the specification limit.

Measurement Algorithm

1 Acquire and split the Read and Write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find tHZEndPoint of the said burst.
4 Find the last falling edge on DQS prior to the tHZEndPoint found.
5 tWPST is the time between the falling DQS edge’s crossings and the tHZEndPoint found.
6 Report tWPST.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.

tWPRE, Write Preamble - Test Method of Implementation

"The purpose of this test is to verify that the time when DQS start driving high (preamble behaviour) to the first DQS signal rising edge crossing for write cycle must be within the conformance limit as specified in the JEDEC specification.

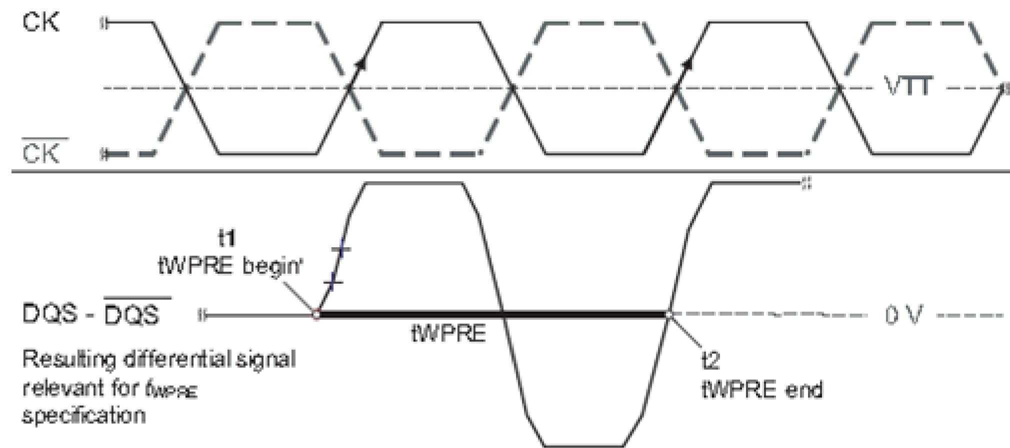


Figure 30 tWPRE Transitions and Endpoints Calculation

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 44 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	tCK(avg)	1

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	tCK(avg)	1

NOTE 1: Please refer to page 160, *JEDEC Standard JESD79- 3*.

PASS Condition

The measured time interval of the point where the DQS starts to transit from tristate (high impedance state to low state) to the DQS signal crossing point for the Write cycle, should be within the specification limit.

Measurement Algorithm

1 Acquire and split the Read and Write bursts of the acquired signal.
2 Take the first valid WRITE burst found.
3 Find tLZBeginPoint of the said burst.
4 Find the first rising edge on DQS of the found burst.
5 tWPRE is the time between the rising DQS edge's crossings and the tLZBeginPoint found.
6 Report tWPRE.

Test References

See Table 65 - Timing Parameters by Bin, in the *JEDEC Standard JESD79- 3C*.

tRPRE, Read Preamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS start driving low (*preamble behavior) to the first DQS signal crossing for the Read cycle must be within the conformance limit as specified in the *JEDEC Standard* specification.

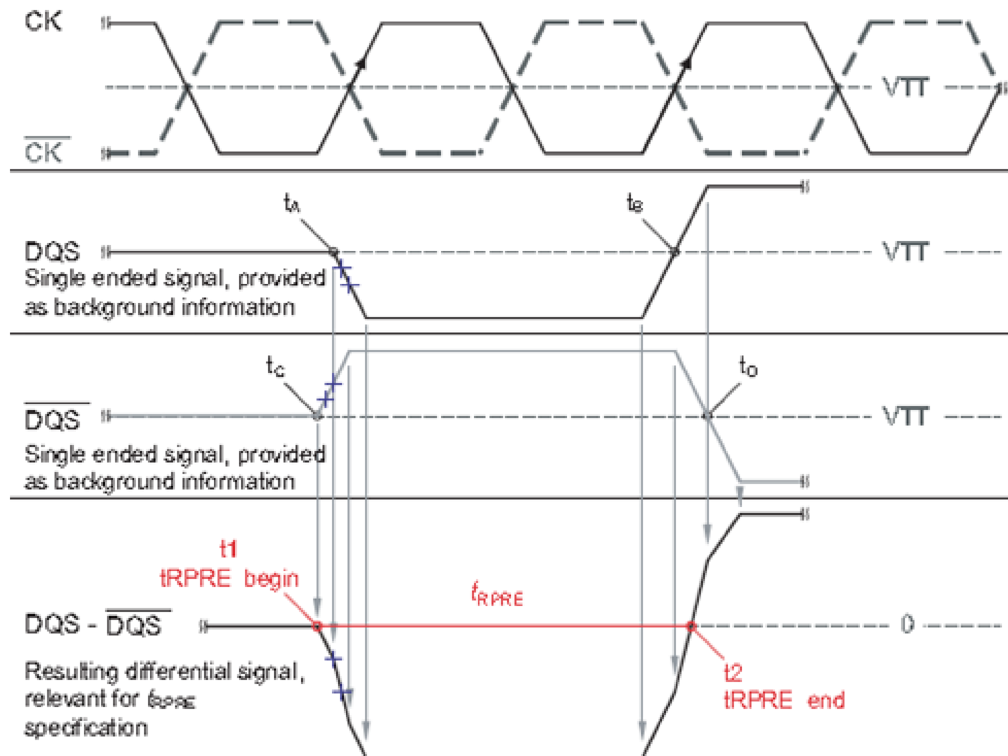


Figure 31 tRPRE Transitions and Endpoints Calculation

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 45 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	tCK(avg)	1,19, g

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	tCK(avg)	1,19, g

NOTE 1,19: Please refer to page 160, *JEDEC Standard JESD79- 3*.

PASS Condition

The measured time interval of the point where the DQS starts to transit from tristate (high impedance state to low state) to the DQS signal crossing point for the Read cycle should be within the specification limit.

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid READ burst found.
3. Find tLZBeginPoint of the said burst.
4. Find the first rising edge on DQS of the found burst.
5. tRPRE is the time between the rising DQS edge and the tLZBeginPoint found.
6. Report tRPRE.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.

tRPST, Read Postamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS is no longer driving (from high/low state to high-impedance) to the last DQS signal crossing (last bit of the data burst) for the Read cycle is within the conformance limit as specified in the JEDEC Specification.

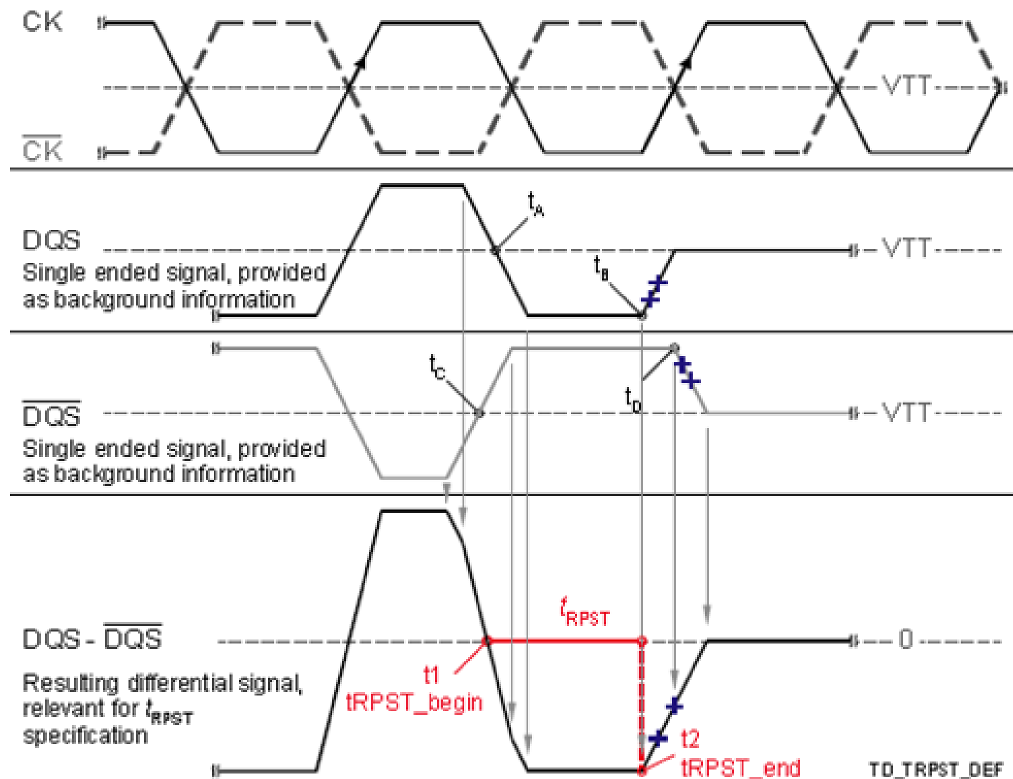


Figure 32 tRPST Transitions and Endpoints Calculation

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (supported by Data Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 46 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	tCK(avg)	11, 13, g

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	tCK(avg)	11, 13, g

NOTE 11, 12,13: Please refer to page 160, *JEDEC Standard JESD79- 3*.

PASS Condition

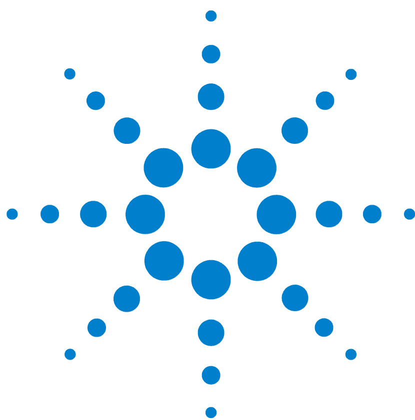
The measured time interval between the last DQS signal crossing point to the point where the DQS starts to transit from high/low level to high impedance for the Read cycle should be within the specification limit.

Measurement Algorithm

1. Acquire and split the Read and Write bursts of the acquired signal.
2. Take the first valid READ burst found.
3. Find tHZEndPoint of the said burst.
4. Find the last falling edge on DQS prior to the tHZEndPoint found.
5. tRPST is the time between the falling DQS edge's crossings and the tHZEndPoint found.
6. Report tRPST.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.



9
Data Timing (DT) Tests

Probing for Data Timing Tests 134
tDS(base), Differential DQ and DM Input Setup Time - Test Method of Implementation 137
tDH(base), Differential DQ and DM Input Hold Time - Test Method of Implementation 140
tDS-Diff(derate), Differential DQ and DM Input Setup Time with Derating Support - Test Method of Implementation 143
tDH-Diff(derate), Differential DQ and DM Input Hold Time with Derating Support - Test Method of Implementation 149
tHZ(DQ), DQ Out High Impedance Time From CK/CK# - Test Method of Implementation 155
tLZ(DQ), DQ Low-Impedance Time from CK/CK# - Test Method of Implementation 157
tDQSQ, DQS-DQ Skew for DQS and Associated DQ Signals - Test Method of Implementation 159
tQH, DQ/DQS Output Hold Time From DQS - Test Method of Implementation 162

This section provides the Methods of Implementation (MOIs) for Data Timing tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

NOTE

Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Data Timing Tests

When performing the Data Timing tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for Data Timing tests may look similar to the following diagrams. Refer to the Connection tab in DDR3 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

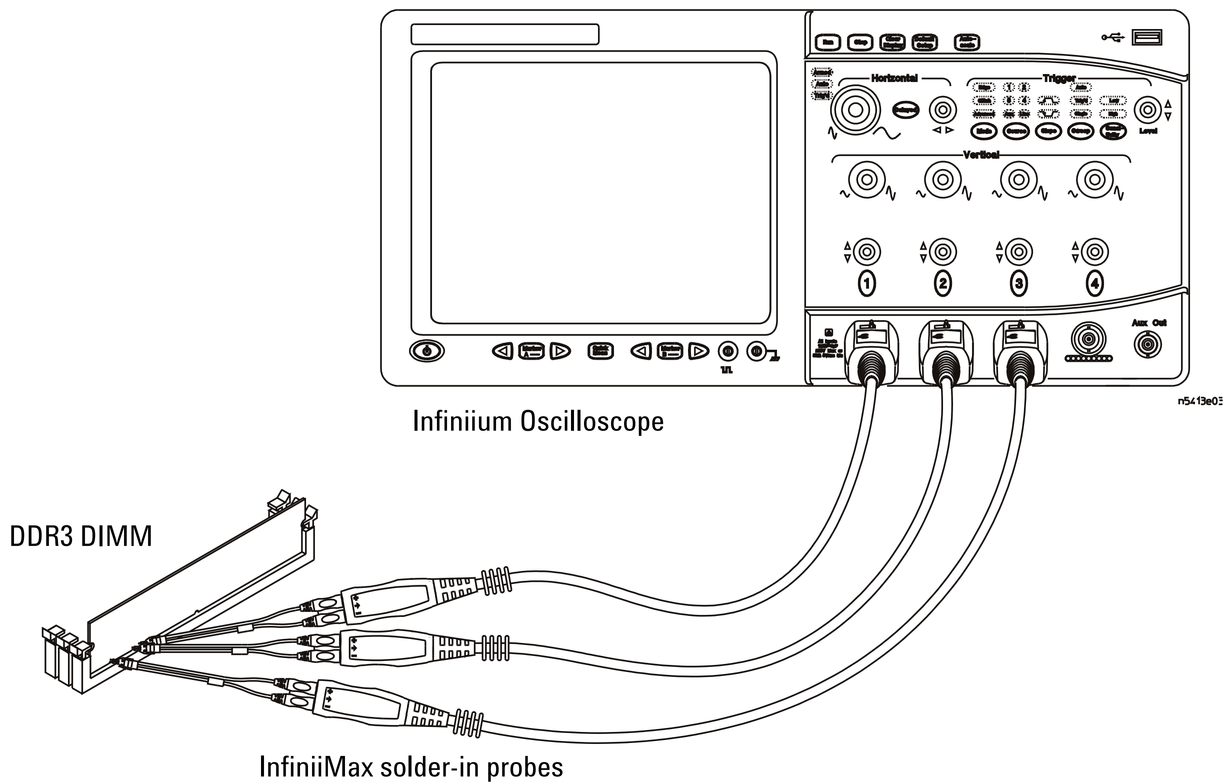


Figure 33 Probing for Data Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 33 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 13, “InfiniiMax Probing,” starting on page 209.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR3 Test application, click the Set Up tab.

6 Select the Speed Grade options. For Data Timing Tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

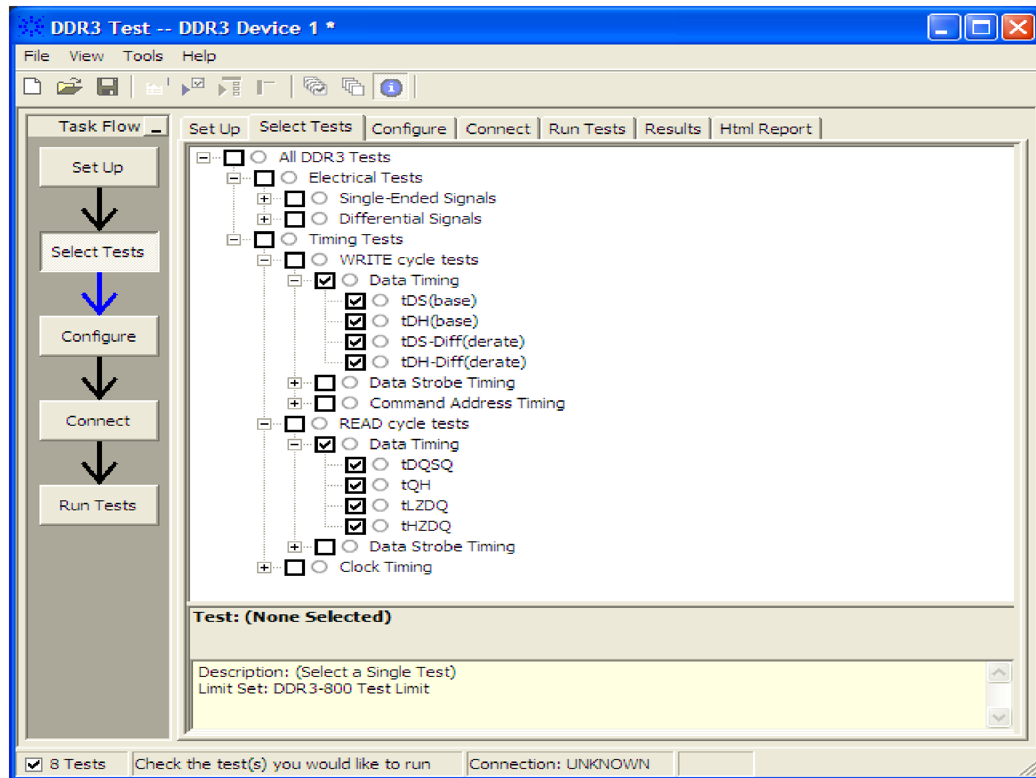


Figure 34 Selecting Data Timing Tests

tDS(base), Differential DQ and DM Input Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling Edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC Specification.

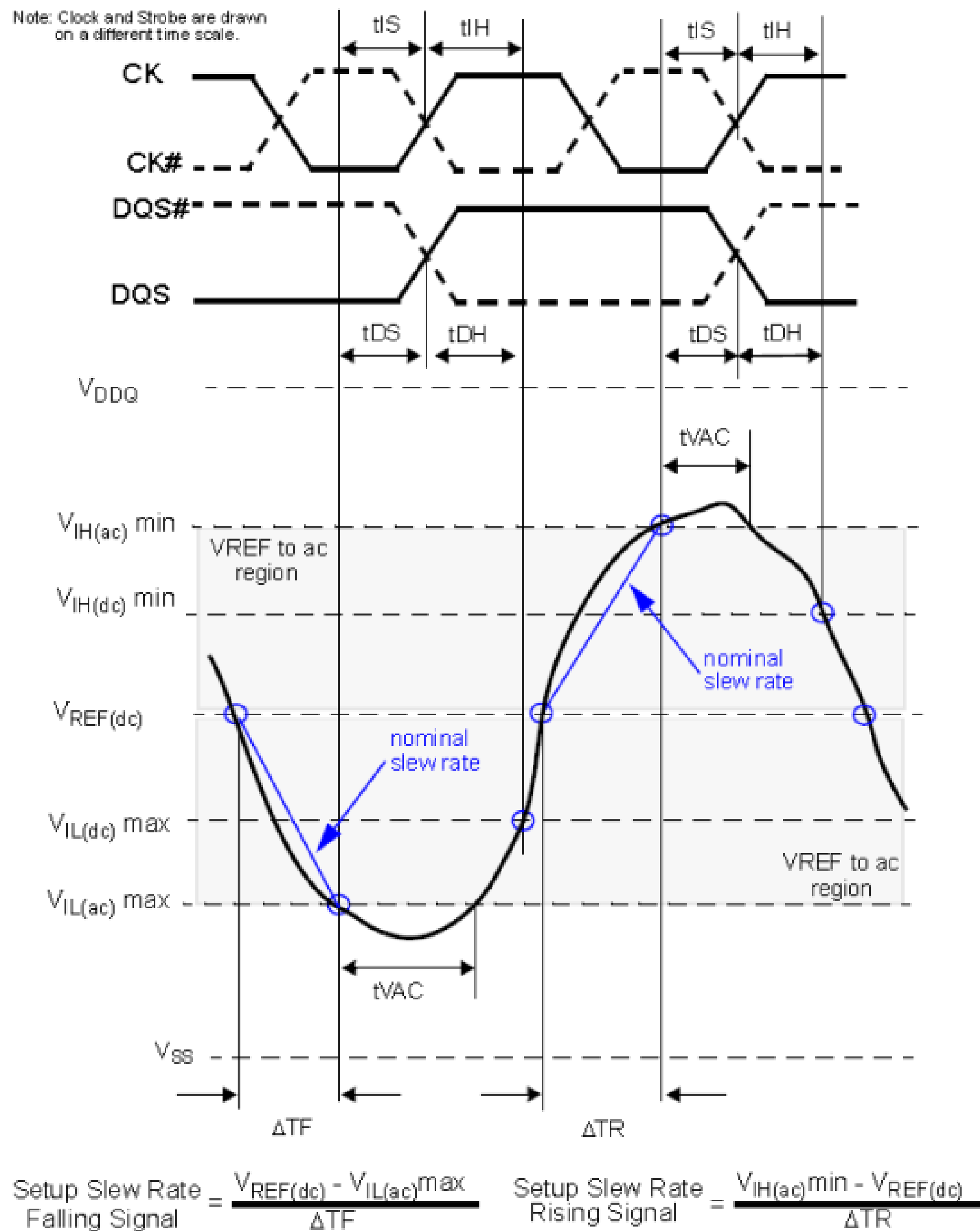


Figure 35 Nominal Slew Rate and t_{VAC} for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (supported by Data Strobe Signal) OR
- Data Mask Signal

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ) or Data Mask Signal (DM)
- Data Strobe Signal (DQS as Supporting Signal)
  - Use differential connection (DQS+ and DQS-)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 47 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Data setup time to DQS, DQS# referenced to Vih(ac), Vil(ac) levels	tDS(base)	75	-	25	-	ps	d, 17

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Data setup time to DQS, DQS# referenced to Vih(ac), Vil(ac) levels	tDS(base)	30	-	10	-	ps	d, 17

NOTE d, 17: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval between the data or data mask (DQ/DM) setup time to the respective DQS crossing point should be within the specification limit.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising DQ crossings that cross Vih(ac) in the said burst.
4. Find all valid falling DQ crossings that cross Vil(ac) in the same burst.
5. For all DQ crossings found, locate all next DQS crossings that cross 0V.
6. tDS is defined as the time between the DQ crossing and the DQS crossing.
7. Collect all tDS.
8. Find the worst tDS among the measured values and report the value as the test result.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.

tDH(base), Differential DQ and DM Input Hold Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the JEDEC Specification.

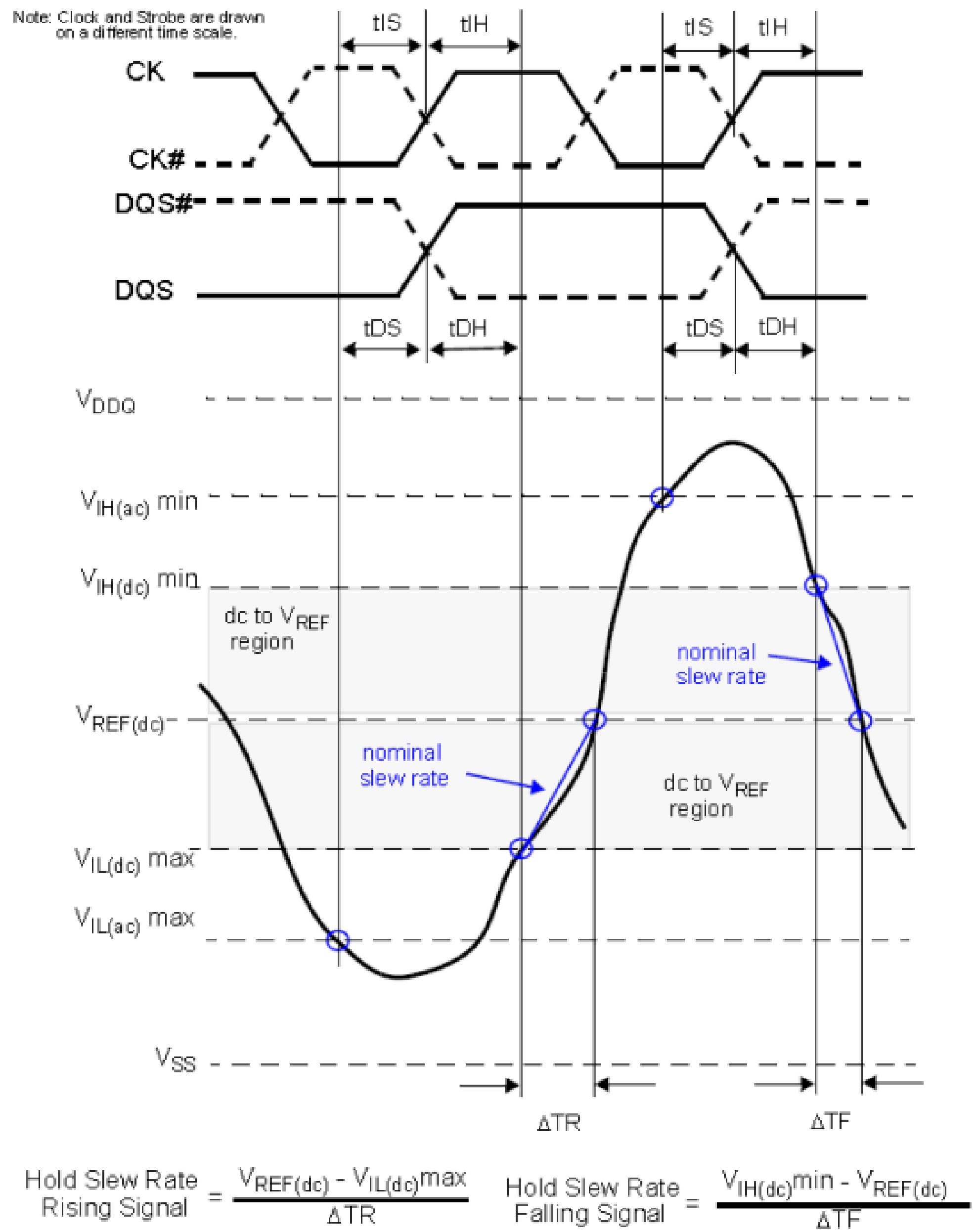


Figure 36 Nominal Slew Rate for Hold Time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock)

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (supported by Data Strobe Signals) OR
- Data Mask Signal

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal) OR Data Mask Signal, DM
- Data Strobe Signal (DQS as Supporting Signal)
  - Use differential connection (DQS+ and DQS-)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 48 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Data hold time from DQS, DQS# referenced to Vih(ac), Vil(ac) levels	tDH(base)	150	-	100	-	ps	d, 17

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Data hold time from DQS, DQS# referenced to Vih(ac), Vil(ac) levels	tDH(base)	65	-	45	-	ps	d, 17

NOTE d, 17: Please refer to page 160, *JEDEC Standard JESD79-3*.

PASS Condition

The measured time interval between the data or data mask (DQ/DM) hold time to the respective DQS crossing point should be within the specification limit.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising DQ crossings that cross $V_{IL(DC)}$ in the said burst.
4. Find all valid falling DQ crossings that cross $V_{IH(DC)}$ in the same burst.
5. For all DQ crossings found, locate all next DQS crossings that cross 0V.
6. tDH is defined as the time between the DQ crossing and the DQS crossing.
7. Collect all tDH.
8. Find the worst tDH among the measured values and report the value as the test result.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.

tDS-Diff(derate), Differential DQ and DM Input Setup Time with Derating Support - Test Method of Implementation

The purpose of this test is to verify that the time interval from data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS crossing edge must be within the conformance limit as specified in the JEDEC Specification.

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (supported by Data Strobe Signal) OR
- Data Mask Signal

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ) or Data Mask Signal (DM)
- Data Strobe Signal (DQS as Supporting Signal)
  - Use differential connection (DQS+ and DQS-)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 49 Data Setup and Hold Base-Values

Units (ps)	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Reference
tDS (base)	75	25	30	10	$V_{IH/L(AC)}$
tDH (base)	150	100	65	45	$V_{IH/L(DC)}$

Table 50 Derating Values DDR3-800/1066 tDS/DH - AC/DC based

ΔtDS, ΔtDH derating in [ps] AC/DC based									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
CMD/ADD Slew Rate V/ns	2.0	88	50	88	50	88	50	-	-
	1.5	59	34	59	34	59	34	67	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	-2	-4	-2	-4	6	4
	0.8	-	-	-	-	-6	-10	2	-2
	0.7	-	-	-	-	-	-	-3	-8
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-
NOTE 1. Empty cell contents are defined as not supported.									

ΔtIS, ΔtIH derating in [ps] AC/DC based									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
CMD/ADD Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	14	12	22	20	-	-	-	-
	0.8	10	6	18	14	26	24	-	-
	0.7	5	0	13	8	21	18	29	34
	0.6	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-30	-26	-22	-10
NOTE 1. Empty cell contents are defined as not supported.									

Table 51 Derating Values DDR3-1333/1600 tDS/DH - AC/DC based

ΔtDS, ΔtDH derating in [ps] AC/DC based									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		**3.0V/ns**		**2.0V/ns**		**1.8V/ns**	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
CMD/ADD Slew Rate V/ns	2.0	75	50	75	50	75	50	-	-
	1.5	50	34	50	34	50	34	58	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	0	-4	-0	-4	8	4
	0.8	-	-	-	-	-0	-10	8	-2
	0.7	-	-	-	-	-	-	8	-8
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-
NOTE 1. Empty cell contents are defined as not supported.									

ΔtIS, ΔtIH derating in [ps] AC/DC based									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		**1.4V/ns**		**1.2V/ns**		**1.0V/ns**	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
CMD/ADD Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	16	12	24	20	-	-	-	-
	0.8	16	6	24	14	32	24	-	-
	0.7	16	0	24	8	32	18	40	34
	0.6	-15	-10	23	-2	31	8	39	24
	0.5	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	7	-26	15	-10
NOTE 1. Empty cell contents are defined as not supported.									

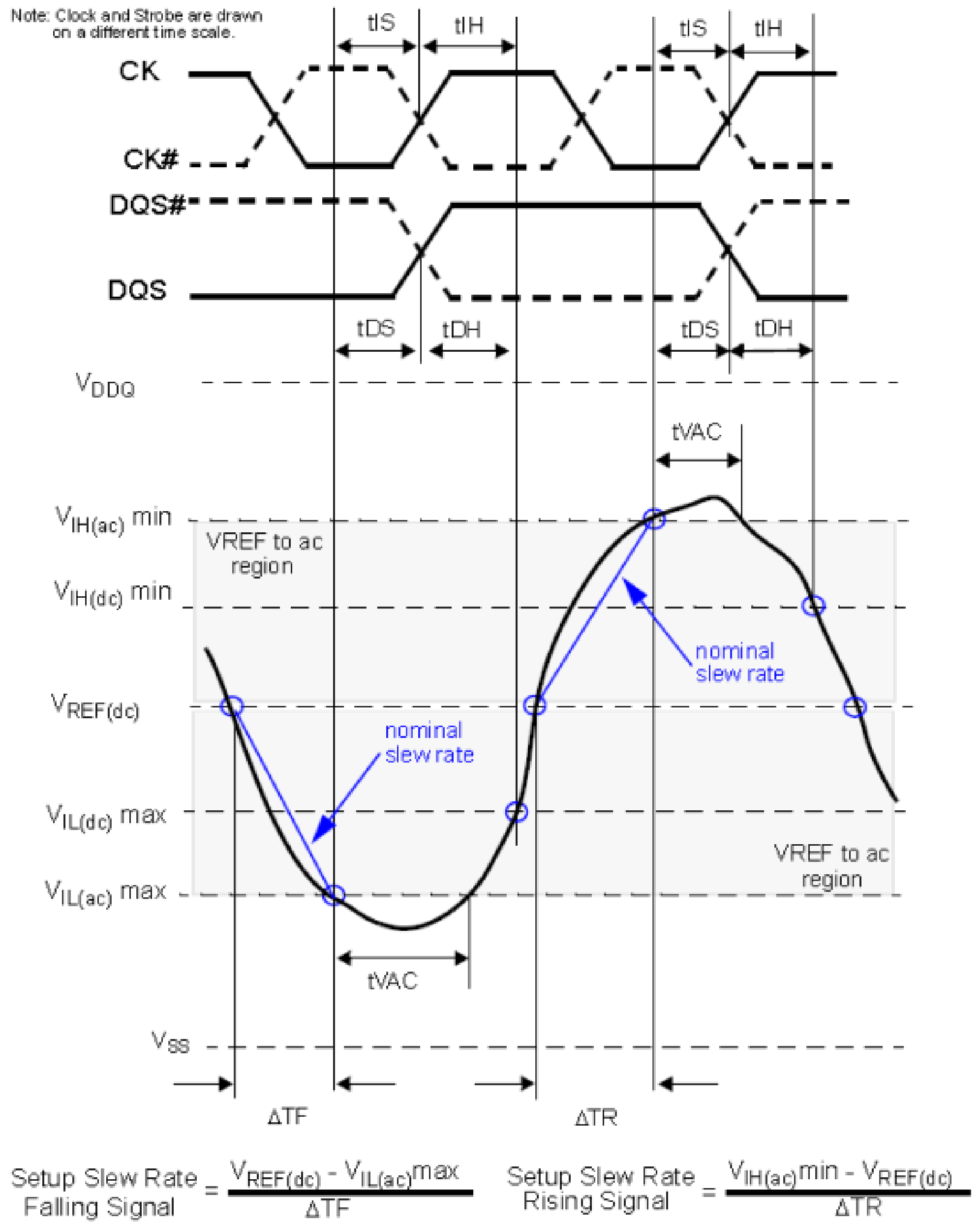


Figure 37 Nominal Slew Rate and t_{VAC} for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

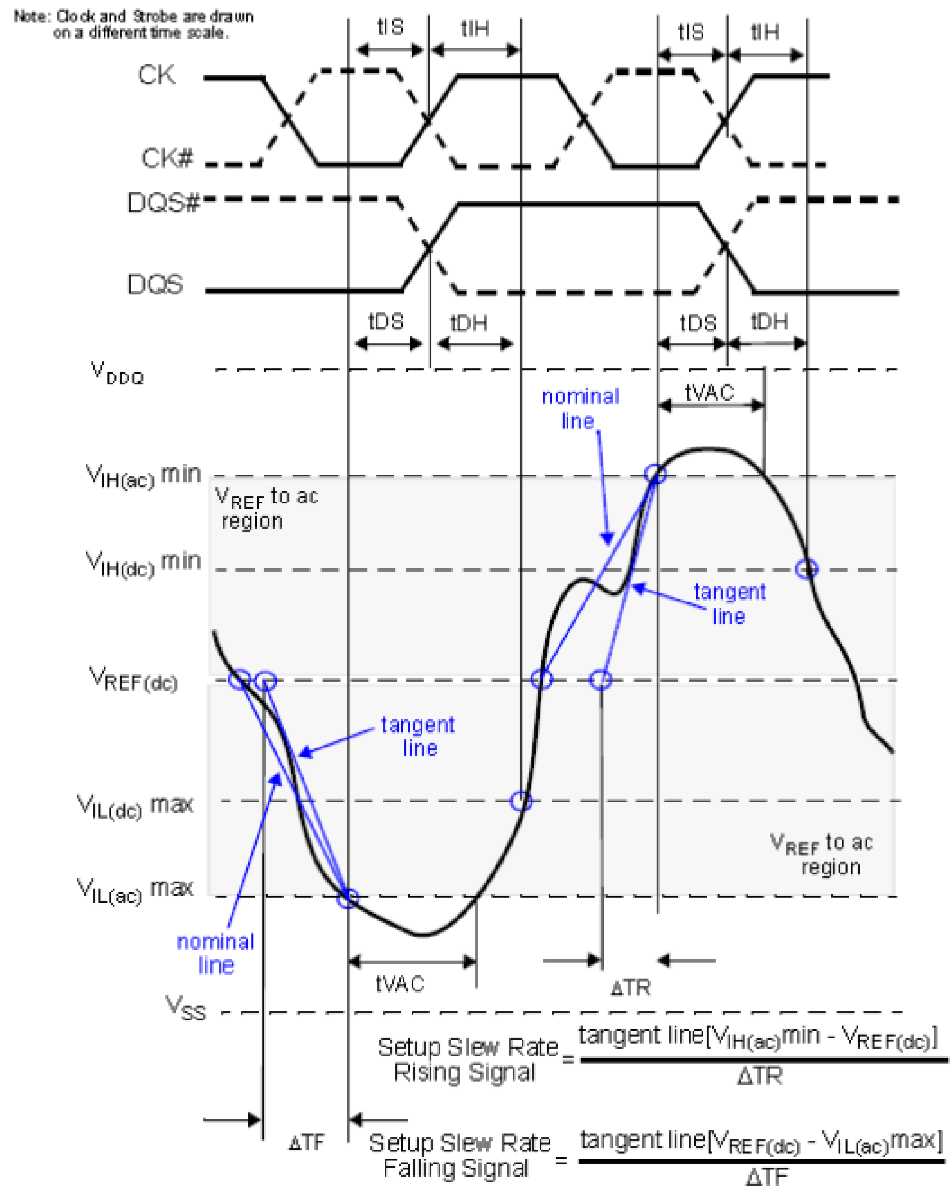


Figure 38 Tangent Line for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

PASS Condition

The measured time interval between the data or data mask (DQ/DM) setup time to the respective DQS crossing point should be within the specification limit.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid WRITE burst found.
3. Find all valid rising DQ crossings that cross VIH(AC) in the said burst.
4. Find all valid falling DQ crossings that cross VIL(AC) in the same burst.
5. For all DQ crossings found, locate all next DQS crossings that cross 0V.
6. tDS is defined as the time between the DQ crossing and the DQS crossing.
7. Collect all tDS.
8. Find the worst tDS among the measured values and report the value as the test result.
9. Measure the mean slew rate for all the DQ and DQS edges.
10. Use the mean slew rate for DQ and DQS to determine the ΔtDS derating value based on the derating tables.
11. The test limit for tDS test = tDS(base) + ΔtDS.

Test References

See Table 70, Table 71 and Table 72 in the *JEDEC Standard JESD79- 3C*.

tDH-Diff(derate), Differential DQ and DM Input Hold Time with Derating Support - Test Method of Implementation

The purpose of this test is to verify that the time interval from data or data mask (DQ/DM rising/falling edge) hold time to the associated DQS crossing edge must be within the conformance limit as specified in the JEDEC Specification.

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (supported by Data Strobe Signals) OR
- Data Mask Signal

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal) OR Data Mask Signal, DM
- Data Strobe Signal (DQS as Supporting Signal)
  - Use differential connection (DQS+ and DQS-)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 52 Data Setup and Hold Base-Values

Units (ps)	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Reference
tDS (base)	75	25	30	10	$V_{IH/L(AC)}$
tDH (base)	150	100	65	45	$V_{IH/L(DC)}$

Table 53 Derating Values DDR3-800/1066 tDS/DH - AC/DC based

ΔtDS, ΔtDH derating in [ps] AC/DC based									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
CMD/ADD Slew Rate V/ns	2.0	88	50	88	50	88	50	-	-
	1.5	59	34	59	34	59	34	67	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	-2	-4	-2	-4	6	4
	0.8	-	-	-	-	-6	-10	2	-2
	0.7	-	-	-	-	-	-	-3	-8
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-
NOTE 1. Empty cell contents are defined as not supported.									

ΔtIS, ΔtIH derating in [ps] AC/DC based									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
CMD/ADD Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	14	12	22	20	-	-	-	-
	0.8	10	6	18	14	26	24	-	-
	0.7	5	0	13	8	21	18	29	34
	0.6	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-30	-26	-22	-10
NOTE 1. Empty cell contents are defined as not supported.									

Table 54 Derating Values DDR3-1333/1600 tDS/DH - AC/DC based

ΔtDS, ΔtDH derating in [ps] AC/DC based									
		DQS, DQS# Differential Slew Rate							
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
CMD/ADD Slew Rate V/ns	2.0	75	50	75	50	75	50	-	-
	1.5	50	34	50	34	50	34	58	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-	-	0	-4	-0	-4	8	4
	0.8	-	-	-	-	-0	-10	8	-2
	0.7	-	-	-	-	-	-	8	-8
	0.6	-	-	-	-	-	-	-	-
	0.5	-	-	-	-	-	-	-	-
	0.4	-	-	-	-	-	-	-	-
NOTE 1. Empty cell contents are defined as not supported.									

ΔtIS, ΔtIH derating in [ps] AC/DC based									
		DQS, DQS# Differential Slew Rate							
		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
CMD/ADD Slew Rate V/ns	2.0	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-	-
	1.0	16	16	-	-	-	-	-	-
	0.9	16	12	24	20	-	-	-	-
	0.8	16	6	24	14	32	24	-	-
	0.7	16	0	24	8	32	18	40	34
	0.6	-15	-10	23	-2	31	8	39	24
	0.5	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	7	-26	15	-10
NOTE 1. Empty cell contents are defined as not supported.									

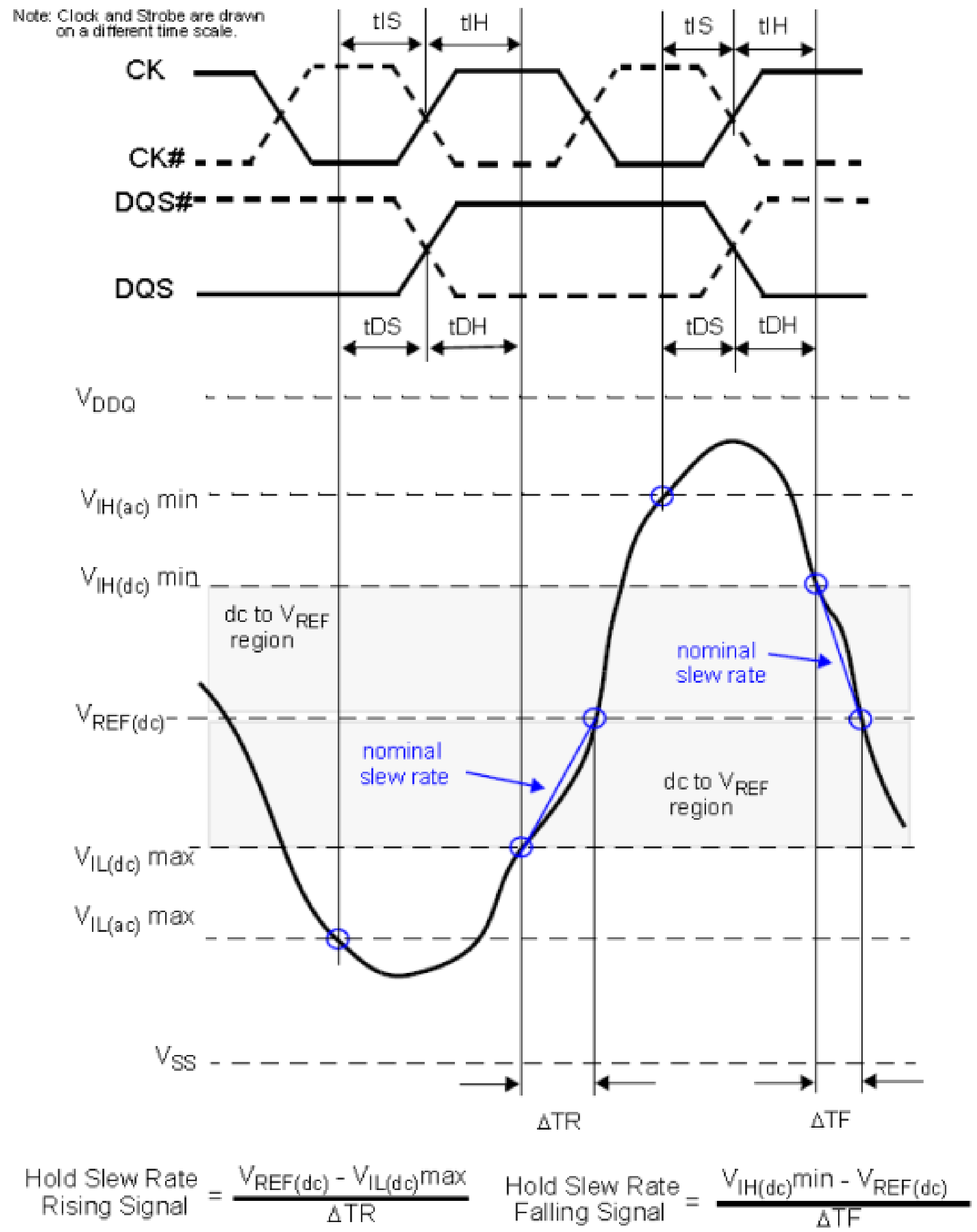


Figure 39 Nominal Slew Rate and t_{VAC} for Hold Time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock)

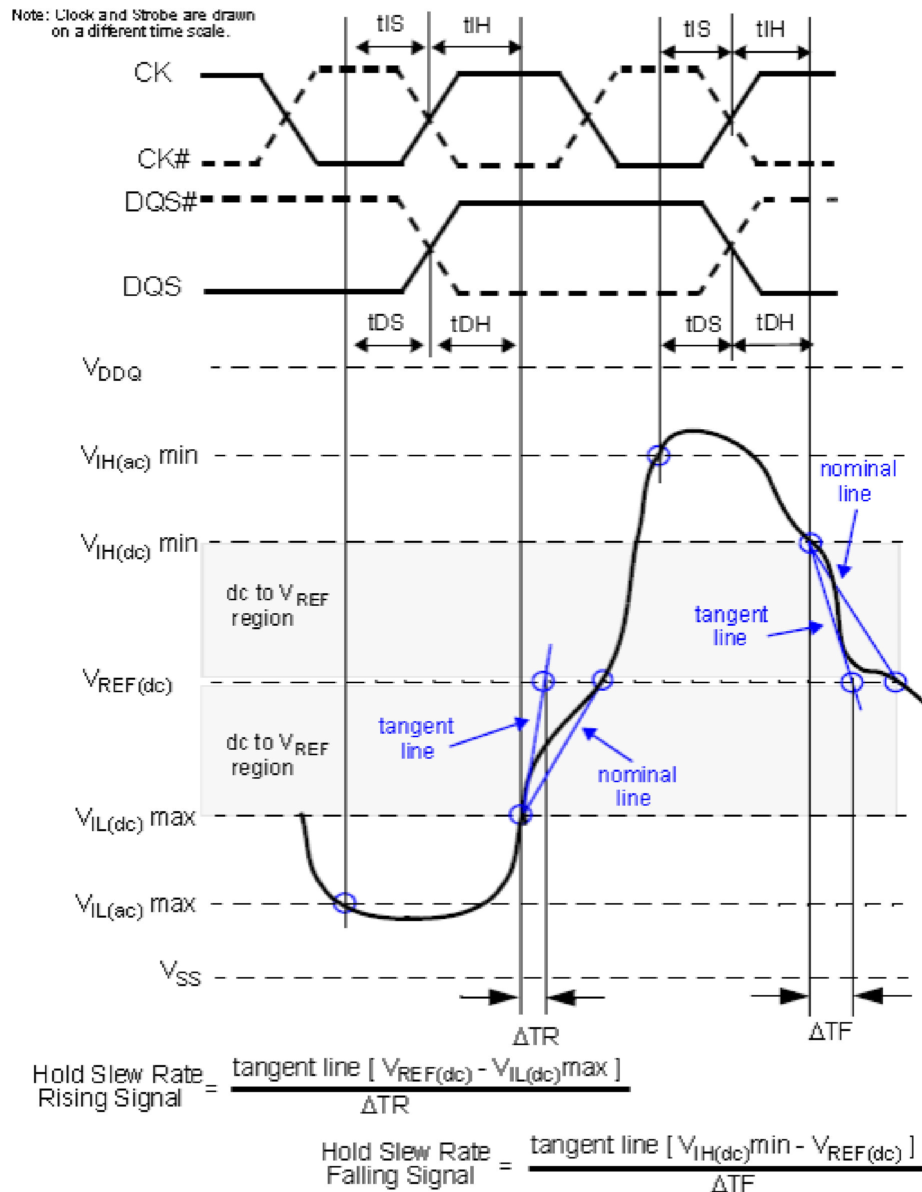


Figure 40 Tangent Line for Hold Time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock)

PASS Condition

The measured time interval between the data or data mask (DQ/DM) hold time to the respective DQS crossing point should be within the specification limit.

Measurement Algorithm

1 Acquire and split Read and Write bursts in the acquired signal.
2 Take the first valid WRITE burst found.
3 Find all valid rising DQ crossings that cross $V_{IL(DC)}$ in the said burst.
4 Find all valid falling DQ crossings that cross $V_{IH(DC)}$ in the same burst.
5 For all DQ crossings found, locate all next DQS crossings that cross 0V.
6 tDH is defined as the time between the DQ crossing and the DQS crossing.
7 Collect all tDH.
8 Find the worst tDH among the measured values and report the value as the test result.
9 Measure the mean slew rate for all the DQ and DQS edges.
10 Use the mean slew rate for DQ and DQS to determine the ΔtDH derating value based on the derating tables.
11 The test limit for tDH test = tDH(base) + ΔtDH.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-3C*.

tHZ(DQ), DQ Out High Impedance Time From CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQ is no longer driving (from high state OR low state to the high impedance stage), to the clock signal crossing, is within the conformance limits as specified in the JEDEC Specification.

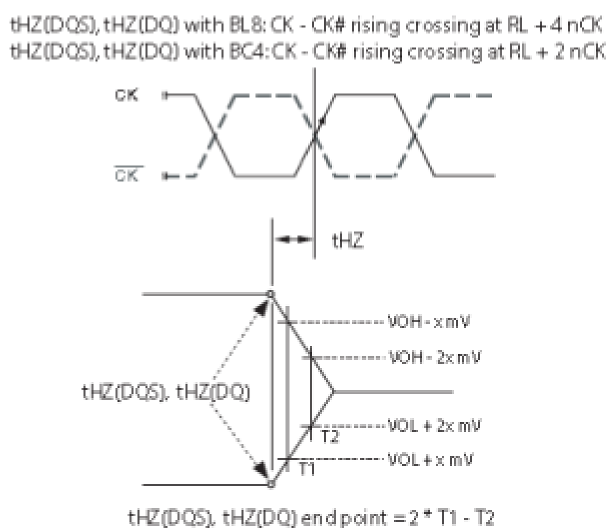


Figure 41 DQ Out High Impedance Time From CK/CK#

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (supported by Data Strobe Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 55 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQ high impedance time from CK/$\overline{CK}$	tHZ(DQ)	-	400	-	300	ps	13,14, f

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQ high impedance time from CK/$\overline{CK}$	tHZ(DQ)	-	250	-	225	ps	13,14, f

NOTE 12,13,14: Please refer to page 160, *JEDEC Standard JESD79- 3*.

PASS Condition

The measured time interval from the point where the DQ starts to transit from high/low state to high impedance state, to the clock signal crossing point should be within the specification limit.

Measurement Algorithm

1 Acquire and split Read and Write bursts in the acquired signal.
2 Take the first valid READ burst found.
3 Find tHZEndPoint of the said burst.
4 Find the nearest Clock rising crossing.
5 tHZ(DQ) is the time interval between the found Clock rising edge's crossing point and the tHZEndPoint.
6 Report tHZ(DQ).

NOTE

Some designs do not have tristate at V_{REF} (for example, 0.9V). This test is not guaranteed when this scenario happens, as there is no significant point of where the driver has been turned-off.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.

tLZ(DQ), DQ Low-Impedance Time from CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQ starts driving (from high impedance state to high/low state), to the clock signal crossing, is within the conformance limit as specified in the JEDEC Specification.

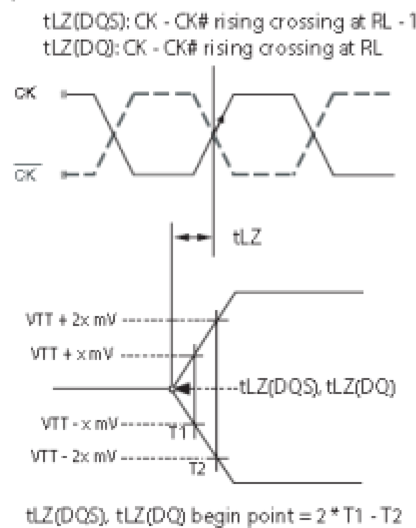


Figure 42 DQ Low-Impedance Time from CK/CK#

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (supported by Data Strobe Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 56 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQ low impedance time from CK/CK#	tLZ(DQ)	-800	400	-600	300	ps	13,14, f

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQ low impedance time from CK/CK#	tLZ(DQ)	-500	250	-450	225	ps	13,14, f

NOTE 12,13,14: Please refer to page 160, *JEDEC Standard JESD79- 3*.

PASS Condition

The measured time interval from the point where the DQ starts to transit from high impedance to the moment when it starts to drive high/low (high impedance state to high/low state), to the clock signal crossing point, should be within the specification limit.

Measurement Algorithm

1 Acquire and split Read and Write bursts in the acquired signal.
2 Take the first valid READ burst found.
3 Find tLZBeginPoint of the said burst.
4 Find the nearest Clock rising crossing.
5 tLZ(DQ) is the time interval between the found Clock rising edge's crossing point and the tLZBeginPoint.
6 Report tLZ(DQ).

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.

tDQSQ, DQS-DQ Skew for DQS and Associated DQ Signals - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS rising and falling edge) access time to the associated data (DQ rising and falling) signal is within the conformance limit as specified in the *JEDEC Standard*.

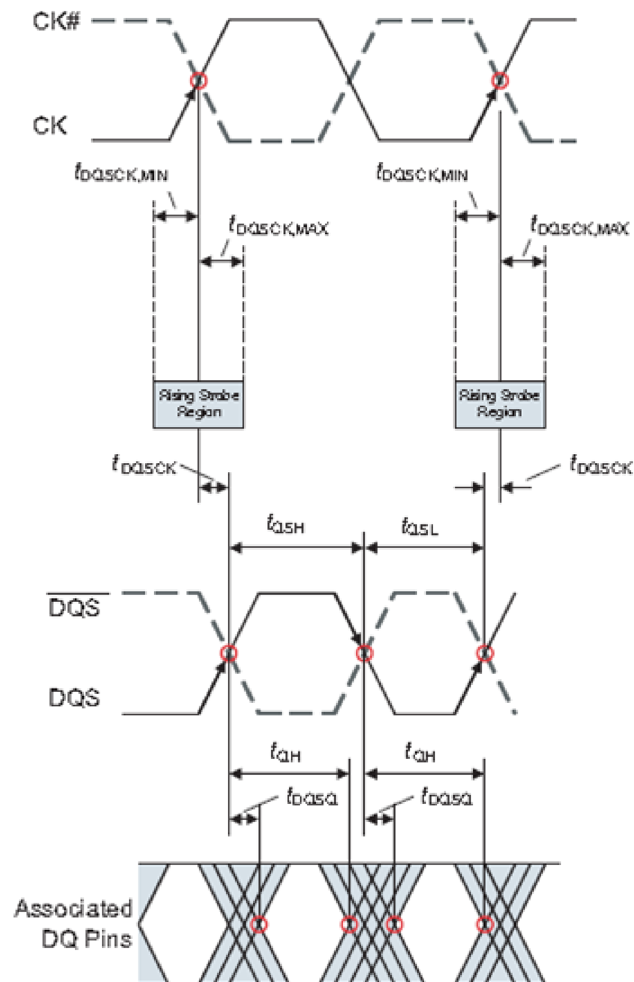


Figure 43 DQS-DQ Skew for DQS and Associated DQ Signals

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 57 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	200	-	150	ps	12,13

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	125	-	100	ps	12,13

NOTE 12,13: Please refer to page 160, *JEDEC Standard JESD79- 3*.

PASS Condition

The measured time interval between the data strobe and the associated data signal should be within specification limit.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid riding and falling DQ crossings at Vref in the said burst.
4. For all DQ crossings found, locate the nearest DQS crossing (rising and falling).
5. Take the time difference between the DQ crossing and DQS crossing as the tDQSQ.
6. Determine the worst result from the set of tDQSQ measured.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.

tQH, DQ/DQS Output Hold Time From DQS - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data output hold time (DQS rising and falling edge) from the DQS (rising and falling edge) is within the conformance limit as specified in the JEDEC Specification.

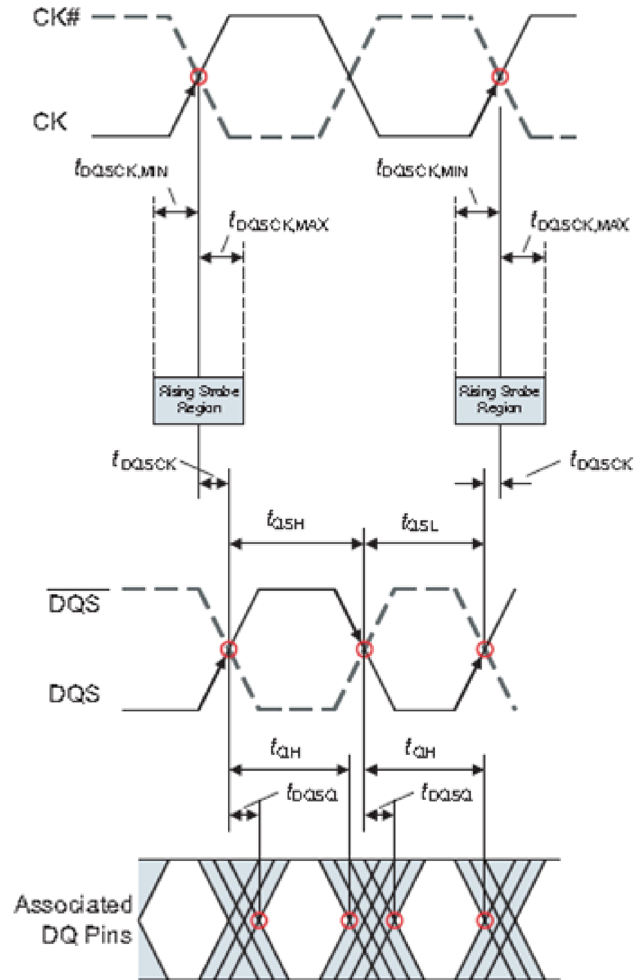


Figure 44 DQ/DQS Output Hold Time From DQS

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 58 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	tCK(avg)	13, g

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	tCK(avg)	13, g

NOTE 12,13: Please refer to page 160, *JEDEC Standard JESD79- 3*.

PASS Condition

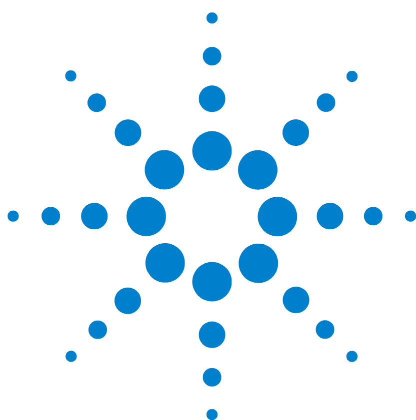
The measured time interval between the data output hold time and the associated data strobe signal should be within specification limit.

Measurement Algorithm

1. Acquire and split Read and Write bursts in the acquired signal.
2. Take the first valid READ burst found.
3. Find all valid riding and falling DQ crossings at Vref in the said burst.
4. For all DQ crossings found, locate the nearest DQS rising crossing.
5. Using the found DQS rising crossing, locate the DQS rising crossing prior.
6. Take the time difference between the DQ crossing and DQS crossing as the tQH.
7. Determine the worst result from the set of tQH measured.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.



10
Command and Address Timing (CAT) Tests

Probing for Command and Address Timing Tests 166
tIS(base) - Address and Control Input Setup Time - Test Method of Implementation 169
tIH(base) - Address and Control Input Hold Time - Test Method of Implementation 172
tIS(derate) - Address and Control Input Setup Time with Derating Support - Test Method of Implementation 175
tIH(derate) - Address and Control Input Hold Time with Derating Support - Test Method of Implementation 180

This section provides the Methods of Implementation (MOIs) for Command and Address Timing tests using an Agilent 80000B or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

NOTE Both XYZ# and $\overline{XYZ}$ are referring to compliment. Thus, CK# is the same as $\overline{CK}$.

Probing for Command and Address Timing Tests

When performing the Command and Address Timing tests, the DDR3 Compliance Test Application will prompt you to make the proper connections. The connection for Command and Address Timing tests may look similar to the following diagrams. Refer to the Connection tab in DDR3 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

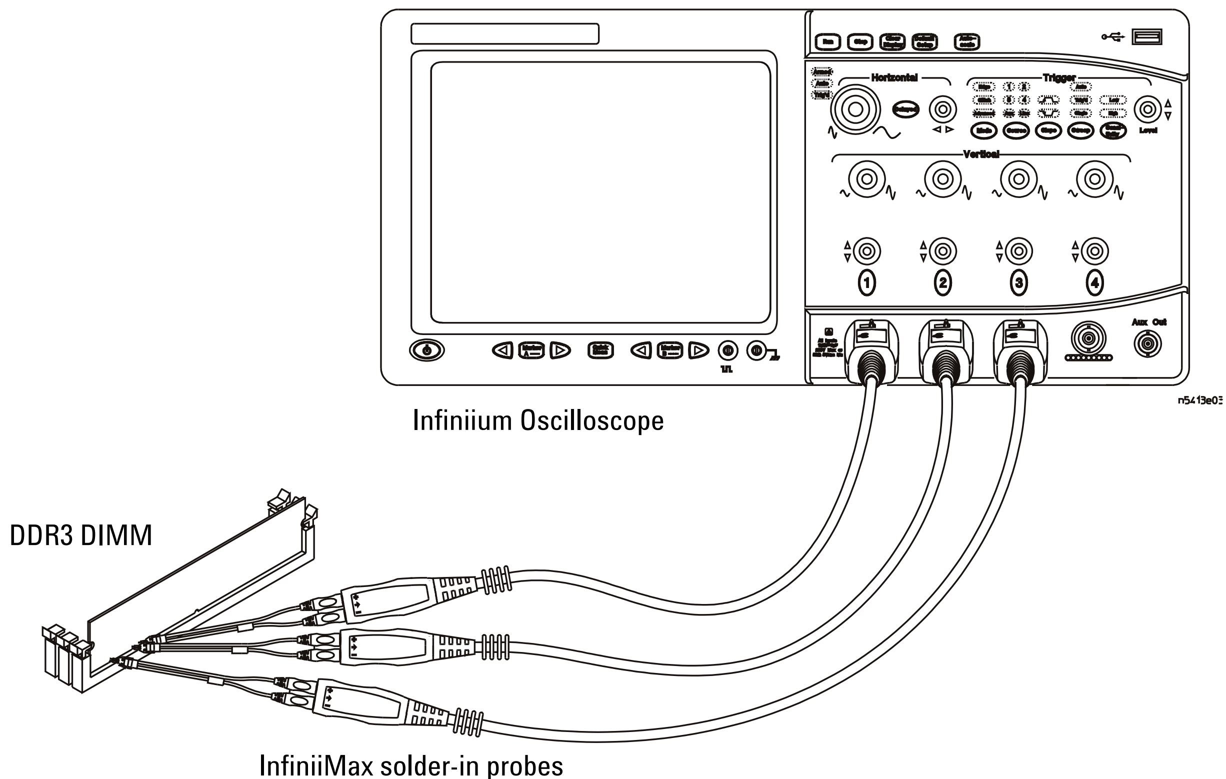


Figure 45 Probing for Command and Address Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 45 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 13, “InfiniiMax Probing,” starting on page 209.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.
2 Ensure that the RAM reliability test software is running on the computer system where the DDR3 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR3 memory.
3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.
4 Connect the oscilloscope probes to any channels of the oscilloscope.
5 In the DDR3 Test application, click the Set Up tab.
6 Select the Speed Grade options. For Command and Address Timing Tests, you can select any speed grade within the selection: DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600.
7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

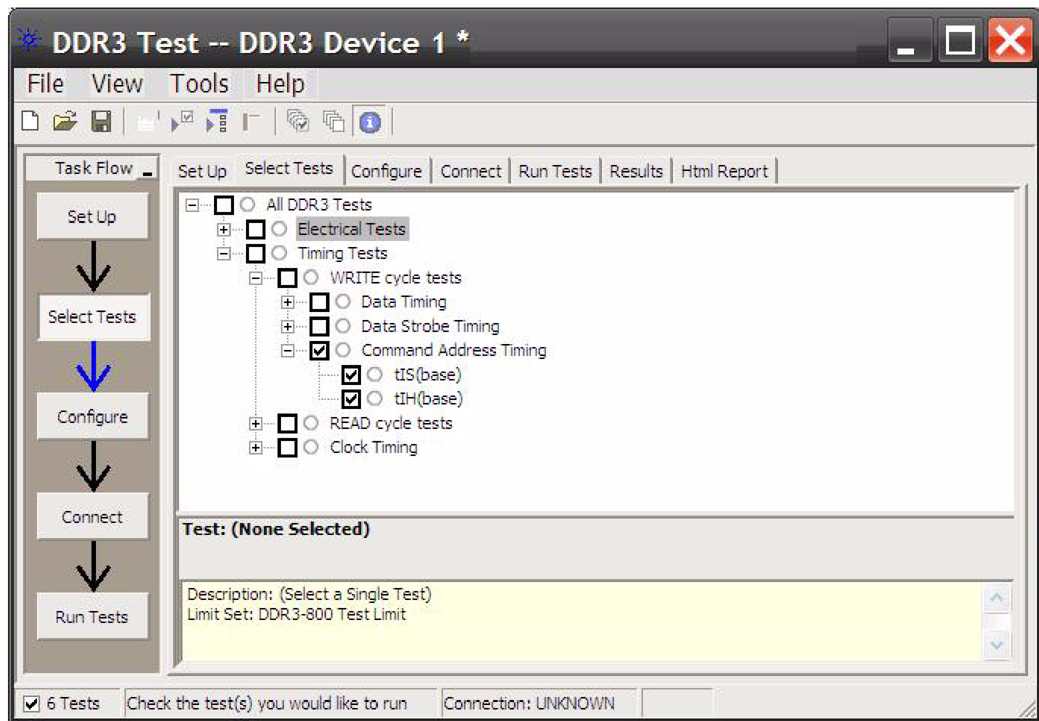


Figure 46 Selecting Command and Address Timing Tests

tIS(base) - Address and Control Input Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control (rising or falling edge) setup time to the associated clock crossing edge is within the conformance limits as specified in the JEDEC Specification.

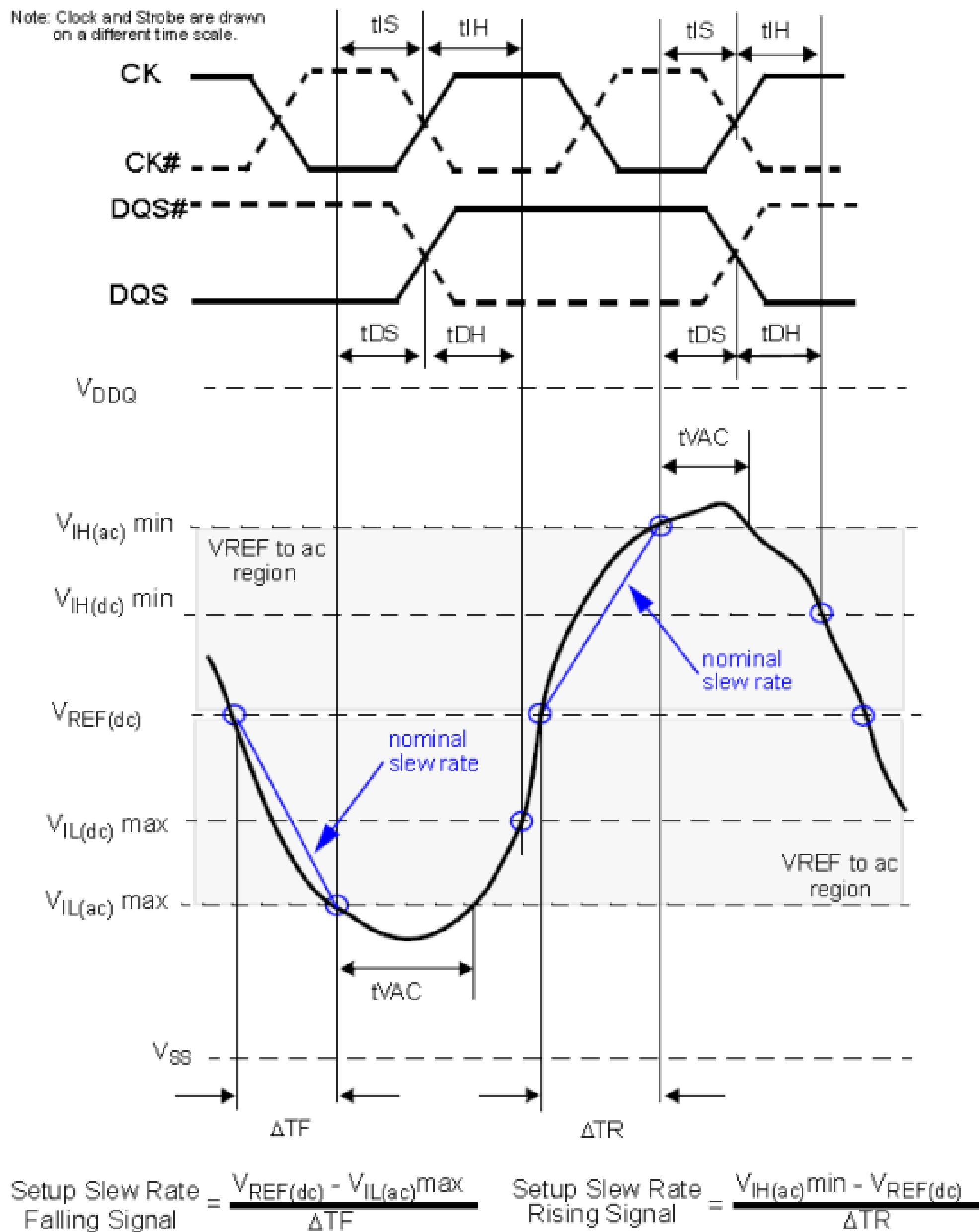


Figure 47 Nominal Slew Rate and t_{VAC} for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

Signals of Interest

Based on the test definition (WRITE cycle only):

- Address or Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Address or Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Test Definition Notes from the Specification

Table 59 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Command and Address setup time to CK, CK# referenced to Vih(ac)/Vil(ac) levels	tIS(base)	200	-	125	-	ps	b, 16

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Command and Address setup time to CK, CK# referenced to Vih(ac)/Vil(ac) levels	tIS(base)	65	-	45	-	ps	b, 16

NOTE b, 16: Please refer to page 160, *JEDEC Standard JESD79- 3*.

PASS Condition

The measured time interval between the address/control setup time and the respective clock crossing point should be within the specification limit.

Measurement Algorithm

1. Precondition the oscilloscope.
2. Trigger on either rising or falling edge of the signal under test that crosses Vih(ac).
3. Find all crossings on rising edge of the signal under test that cross Vih(ac).
4. Find all crossings on falling edge of the signal under test that cross Vil(ac).
5. For all crossings found, locate the nearest Clock crossing that crosses 0V.

6. Take the time difference between the signal under test's crossing and the corresponding clock crossing as tIS.
7. Collect all measured tIS.
8. Report the worst tIS measured as the test result.
9. Compare the test result against the compliance test limit.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.

tIH(base) - Address and Control Input Hold Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control (rising or falling edge) hold time to the associated clock crossing edge is within the conformance limits as specified in the JEDEC Specification.

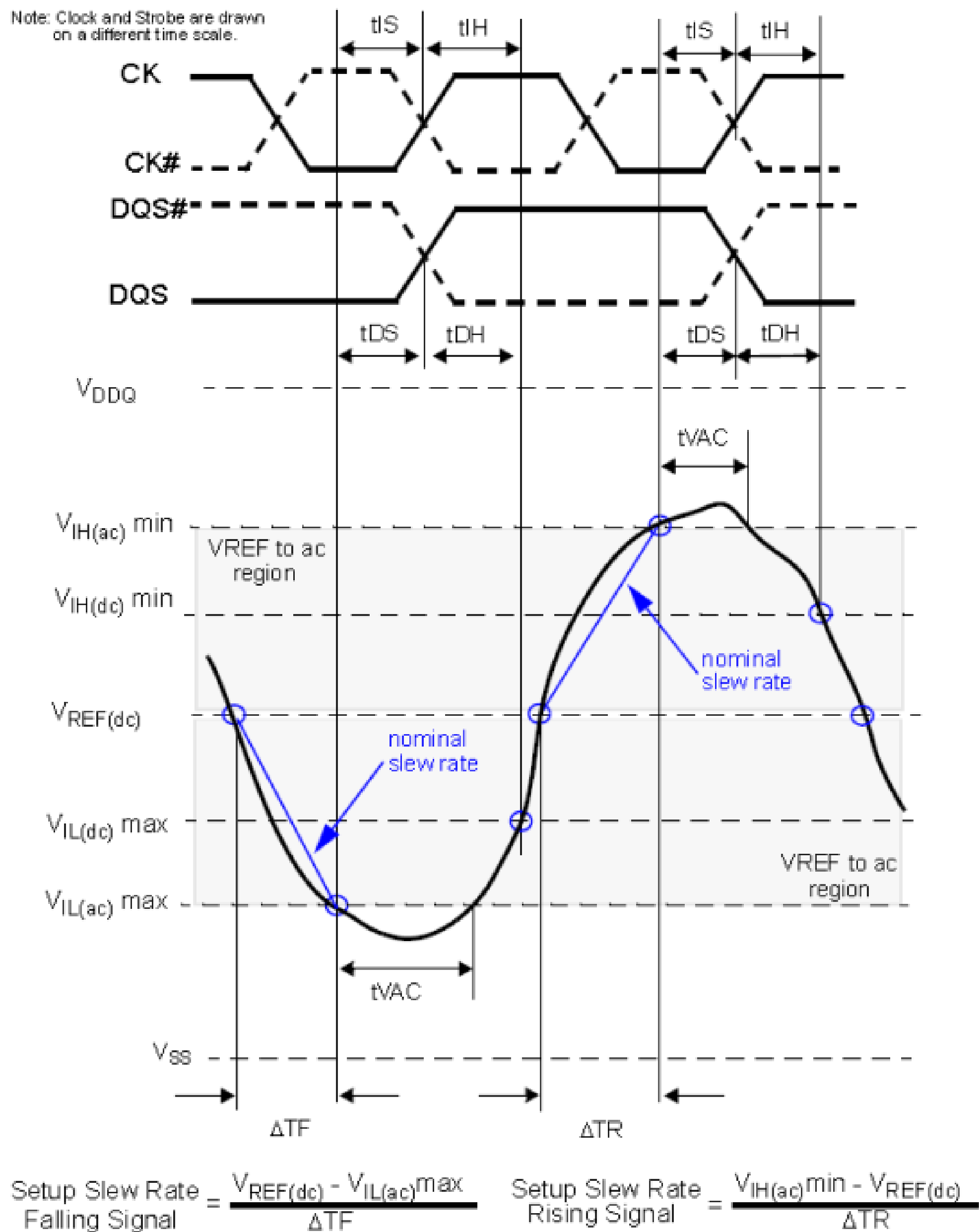


Figure 48 Nominal Slew Rate and t_{VAC} for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

Signals of Interest

Based on the test definition (WRITE cycle only):

- Address or Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Address or Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Test Definition Notes from the Specification

Table 60 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Specific Notes
		Min	Max	Min	Max		
Command and Address hold time to CK, CK# referenced to Vih(ac)/Vil(ac) levels	tIH(base)	275	-	200	-	ps	b, 16

Parameter	Symbol	DDR3-1333		DDR3-1600		Units	Specific Notes
		Min	Max	Min	Max		
Command and Address hold time to CK, CK# referenced to Vih(ac)/Vil(ac) levels	tIH(base)	140	-	120	-	ps	b, 16

NOTE b, 16: Please refer to page 160, *JEDEC Standard JESD79- 3*.

PASS Condition

The measured time interval between the address/control hold time and the respective clock crossing point should be within the specification limit.

Measurement Algorithm

1. Precondition the oscilloscope.
2. Trigger on either rising or falling edge of the address/control signal under test that crosses $V_{IH(AC)}$.
3. Find all crossings on rising edge of the signal under test that cross $V_{IL(DC)}$.
4. Find all crossings on falling edge of the signal under test that cross $V_{IH(DC)}$.
5. For all crossings found, locate the nearest Clock crossing that crosses 0V.

6 Take the time difference between the signal under test's crossing and the corresponding clock crossing as tIH.
7 Collect all measured tIH.
8 Report the worst tIH measured as the test result.
9 Compare the test result against the compliance test limit.

Test References

See Table 65 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79- 3C*.

tIS(derate) - Address and Control Input Setup Time with Derating Support - Test Method of Implementation

The purpose of this test is to verify that the time interval from address or control (Address/Control rising/falling edge) setup time to the associated clock crossing edge must be within the conformance limit as specified in the JEDEC Specification.

Signals of Interest

Based on the test definition (WRITE cycle only):

- Address or Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Address or Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Test Definition Notes from the Specification

Table 61 ADD/CMD Setup and Hold Base-Values for 1V/ns

Units (ps)	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Reference
tIS (base)	200	125	65	45	$V_{IH/L(AC)}$
tIH (base)	275	200	140	120	$V_{IH/L(DC)}$

Table 62 Derating Values DDR3-800/1066/1333/1600 tIS/IH - AC/DC based

ΔtIS, ΔtIH derating in [ps] AC/DC based **AC175 Threshold** → VIH(AC) = VREF(DC) + 175mV, VIL(AC) = VREF(DC) - 175mV									
		CK, CK# Differential Slew Rate							
		4.0V/ns		**3.0V/ns**		**2.0V/ns**		**1.8V/ns**	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	88	50	88	50	88	50	96	58
	1.5	59	34	59	34	59	34	67	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-2	-4	-2	-4	-2	-4	6	4
	0.8	-6	-10	-6	-10	-6	-10	2	-2
	0.7	-11	-16	-11	-16	-11	-16	-3	-8
	0.6	-17	-26	-17	-26	-17	-26	-9	-18
	0.5	-35	-40	-35	-40	-35	-40	-27	-32
	0.4	-62	-60	-62	-60	-62	-60	-54	-52

ΔtIS, ΔtIH derating in [ps] AC/DC based **AC175 Threshold** → VIH(AC) = VREF(DC) + 175mV, VIL(AC) = VREF(DC) - 175mV									
		CK, CK# Differential Slew Rate							
		1.6V/ns		**1.4V/ns**		**1.2V/ns**		**1.0V/ns**	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	104	66	112	74	120	84	128	100
	1.5	75	50	83	58	91	68	99	84
	1.0	16	16	24	24	32	34	40	50
	0.9	14	12	22	20	30	30	38	46
	0.8	10	6	18	14	26	24	34	40
	0.7	5	0	13	8	21	18	29	34
	0.6	-1	-10	7	-2	15	8	23	24
	0.5	-19	-24	-11	-16	-2	-6	5	10
	0.4	-46	-44	-38	-36	-30	-26	-22	-10

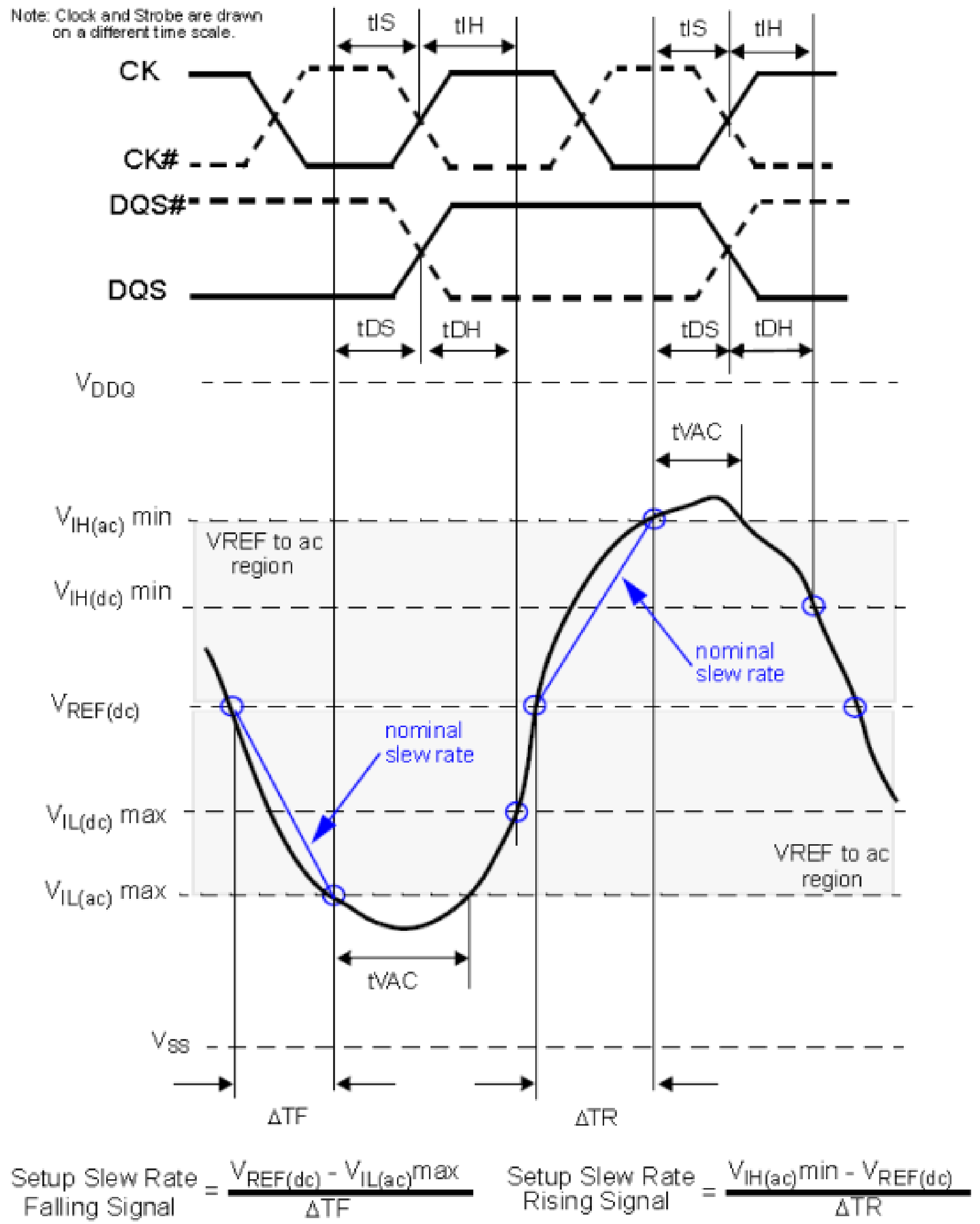


Figure 49 Nominal Slew Rate and t_{VAC} for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

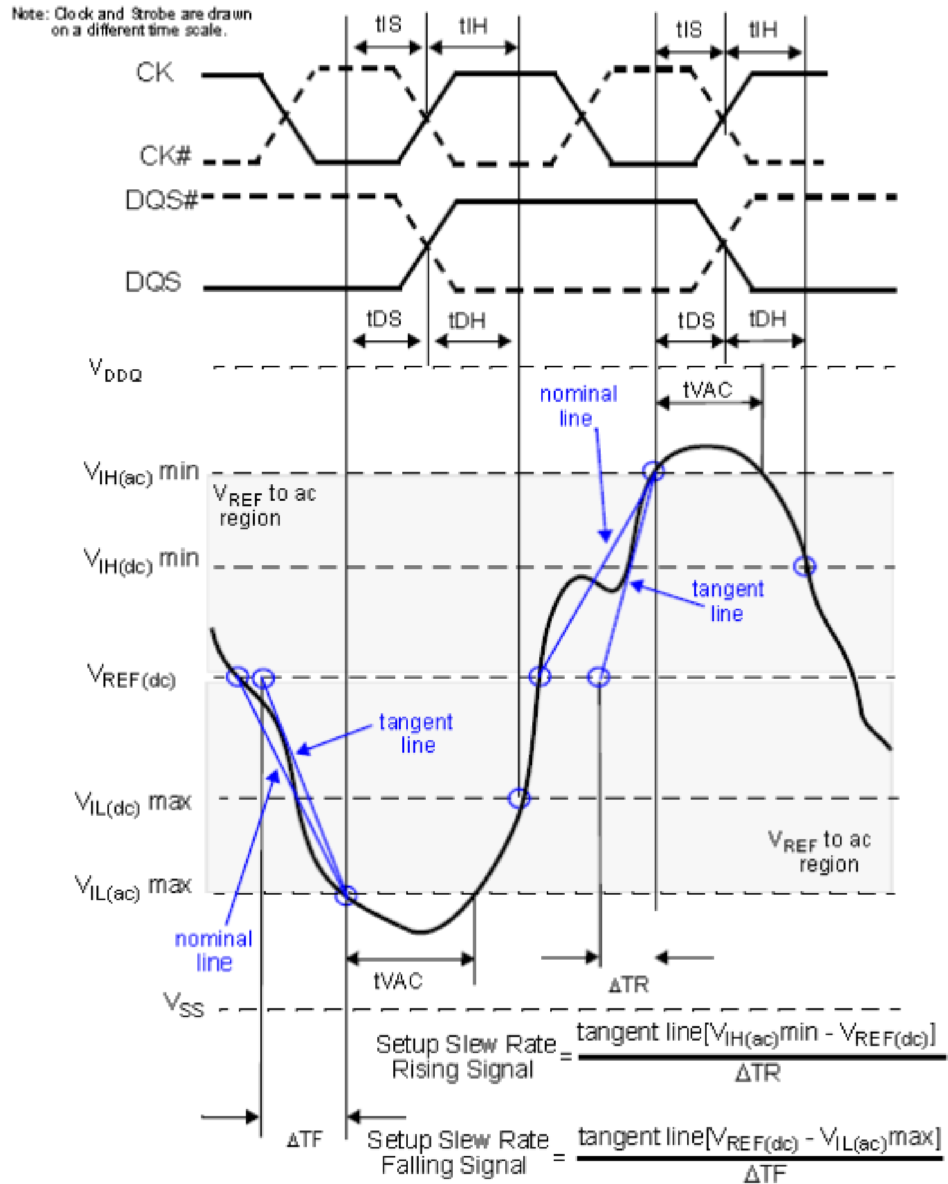


Figure 50 Tangent Line for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

PASS Condition

The measured time interval between address/control setup time to respective clock crossing point shall be within the specification limit.

Measurement Algorithm

1 Precondition the oscilloscope.
2 Trigger on either rising or falling edge of the address/control signal under test.
3 Find all crossings on rising edge of the signal under test that cross $V_{IH(AC)}$.
4 Find all crossings on falling edge of the signal under test that cross $V_{IH(AC)}$.
5 For all crossings found, locate the nearest Clock crossing that crosses 0V.
6 Take the time difference between the signal under test's crossing and the corresponding clock crossing as tIS.
7 Collect all measured tIS.
8 Report the worst tIS measured as the test result.
9 Measure the mean slew rate for all the ADD/CMD and CK edges.
10 Use the mean slew rate for ADD/CMD and CK to determine the ΔtIS derating value based on the derating tables.
11 The test limit for tIS test = tIS(base) + ΔtIS.

Test References

See Table 66 - ADD/CMD Setup and Hold Base-Values for 1V/ns and Table 67 - Derating Values DDR3-800/1066/1333/1600 tIS/IH - AC/DC based, in the *JEDEC Standard JESD79-3C*.

tIH(derate) - Address and Control Input Hold Time with Derating Support - Test Method of Implementation

The purpose of this test is to verify that the time interval from address or control (Address/Control rising/falling edge) hold time to the associated clock crossing edge must be within the conformance limit as specified in the JEDEC Specification.

Signals of Interest

Based on the test definition (WRITE cycle only):

- Address or Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Address or Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Test Definition Notes from the Specification

Table 63 ADD/CMD Setup and Hold Base-Values for 1V/ns

Units (ps)	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Reference
tIS (base)	200	125	65	45	$V_{IH/L(AC)}$
tIH (base)	275	200	140	120	$V_{IH/L(DC)}$

Table 64 Derating Values DDR3-800/1066/1333/1600 tIS/IH - AC/DC based

ΔtIS, ΔtIH derating in [ps] AC/DC based **AC175 Threshold** → VIH(AC) = VREF(DC) + 175mV, VIL(AC) = VREF(DC) - 175mV									
		CK, CK# Differential Slew Rate							
		4.0V/ns		**3.0V/ns**		**2.0V/ns**		**1.8V/ns**	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	88	50	88	50	88	50	96	58
	1.5	59	34	59	34	59	34	67	42
	1.0	0	0	0	0	0	0	8	8
	0.9	-2	-4	-2	-4	-2	-4	6	4
	0.8	-6	-10	-6	-10	-6	-10	2	-2
	0.7	-11	-16	-11	-16	-11	-16	-3	-8
	0.6	-17	-26	-17	-26	-17	-26	-9	-18
	0.5	-35	-40	-35	-40	-35	-40	-27	-32
	0.4	-62	-60	-62	-60	-62	-60	-54	-52

ΔtIS, ΔtIH derating in [ps] AC/DC based **AC175 Threshold** → VIH(AC) = VREF(DC) + 175mV, VIL(AC) = VREF(DC) - 175mV									
		CK, CK# Differential Slew Rate							
		1.6V/ns		**1.4V/ns**		**1.2V/ns**		**1.0V/ns**	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ADD Slew Rate V/ns	2.0	104	66	112	74	120	84	128	100
	1.5	75	50	83	58	91	68	99	84
	1.0	16	16	24	24	32	34	40	50
	0.9	14	12	22	20	30	30	38	46
	0.8	10	6	18	14	26	24	34	40
	0.7	5	0	13	8	21	18	29	34
	0.6	-1	-10	7	-2	15	8	23	24
	0.5	-19	-24	-11	-16	-2	-6	5	10
	0.4	-46	-44	-38	-36	-30	-26	-22	-10

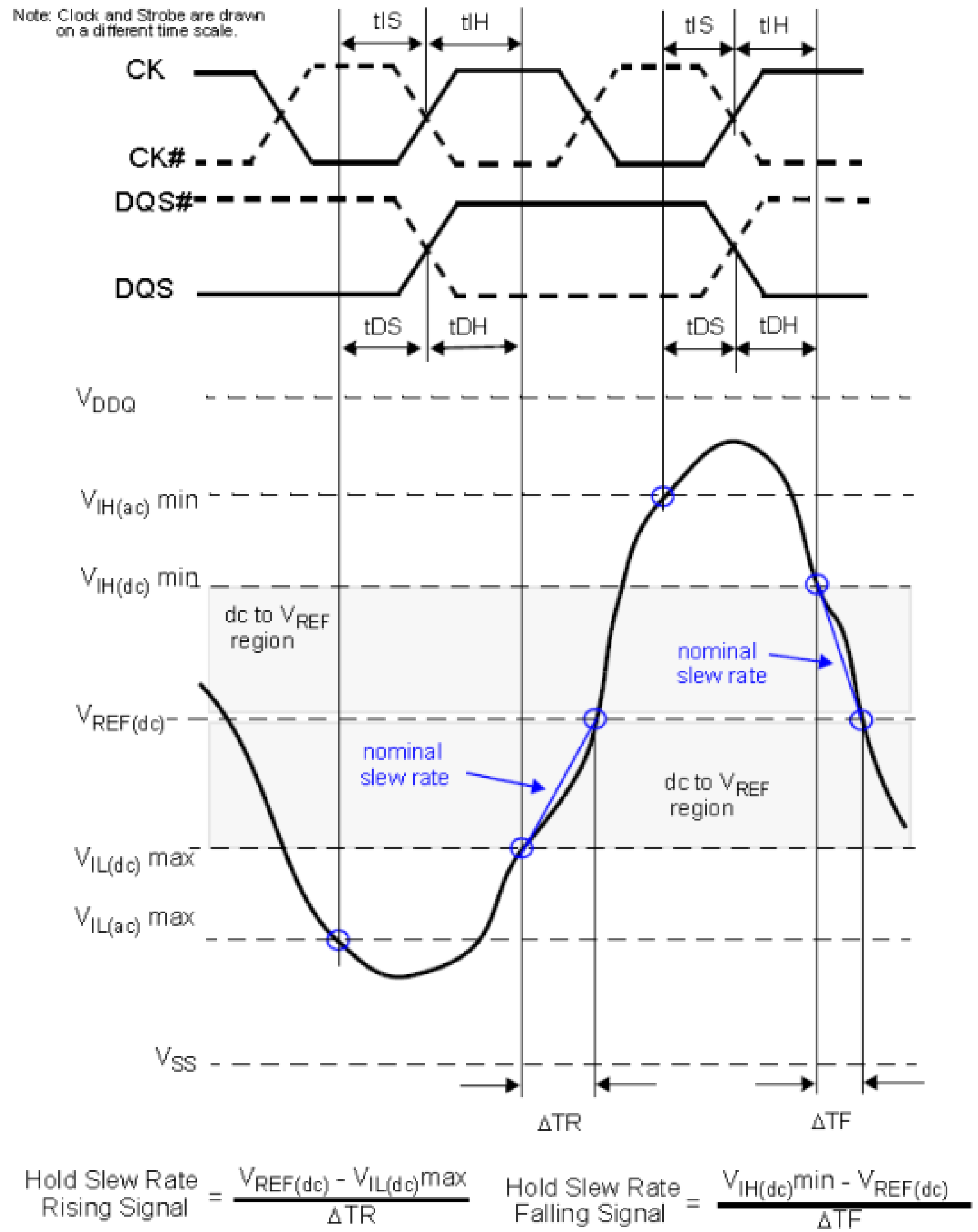


Figure 51 Nominal Slew Rate and t_{VAC} for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

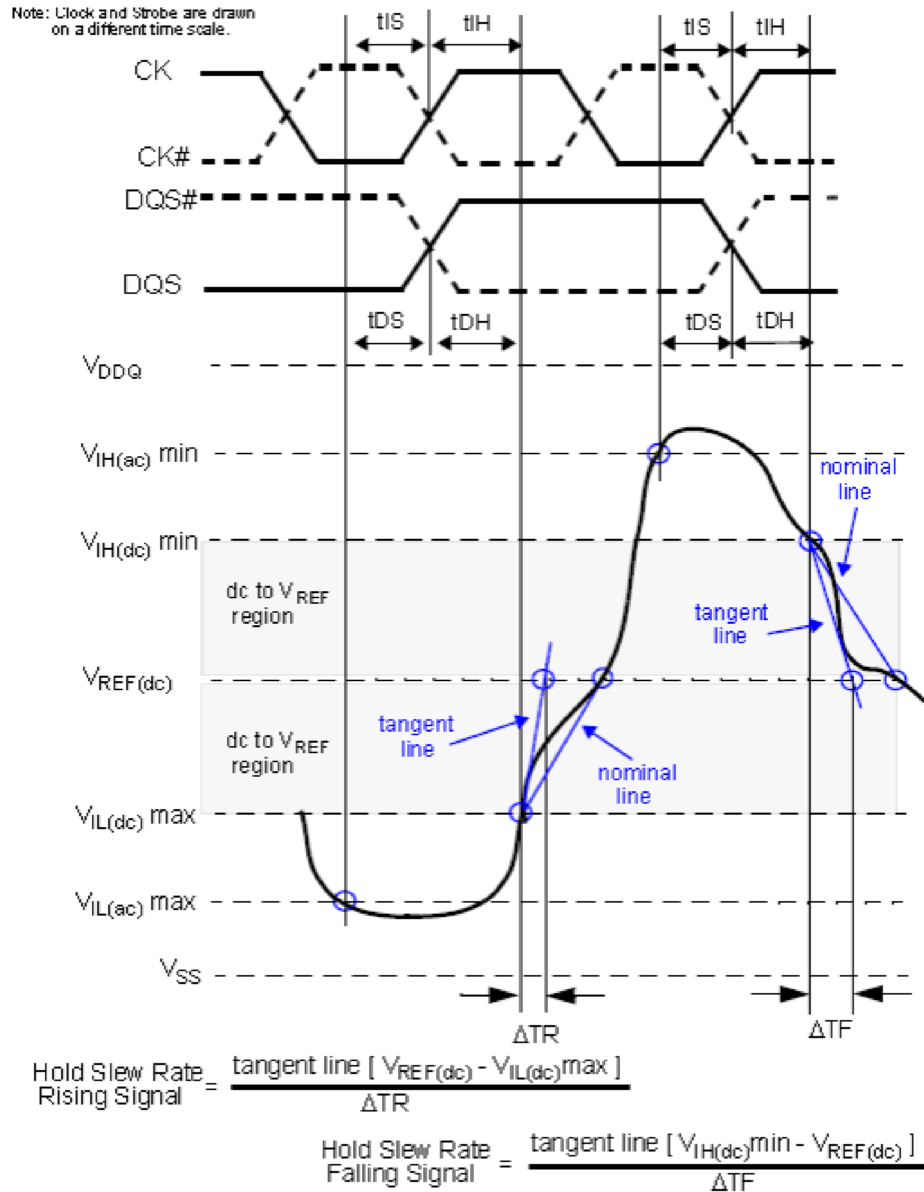


Figure 52 Tangent Line for Setup Time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

PASS Condition

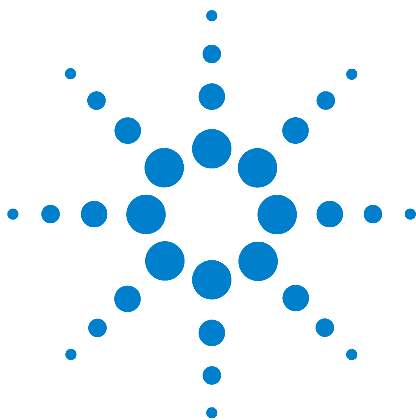
The measured time interval between address/control hold time to respective clock crossing point shall be within the specification limit.

Measurement Algorithm

1. Precondition the oscilloscope.
2. Trigger on either rising or falling edge of the address/control signal under test.
3. Find all crossings on rising edge of the signal under test that cross $V_{IL(DC)}$.
4. Find all crossings on falling edge of the signal under test that cross $V_{IH(DC)}$.
5. For all crossings found, locate the nearest Clock crossing that crosses 0V.
6. Take the time difference between the signal under test's crossing and the corresponding clock crossing as tIH.
7. Collect all measured tIH.
8. Report the worst tIH measured as the test result.
9. Measure the mean slew rate for all the ADD/CMD and CK edges.
10. Use the mean slew rate for ADD/CMD and CK to determine the ΔtIH derating value based on the derating tables.
11. The test limit for tIH test = tIH(base) + ΔtIH.

Test References

See Table 66 - ADD/CMD Setup and Hold Base-Values for 1V/ns and Table 67 - Derating Values DDR3-800/1066/1333/1600 tIS/IH - AC/DC based, in the *JEDEC Standard JESD79-3C*.



11 Custom Mode Read-Write Eye-Diagram Tests

Probing for Custom Mode Read-Write Eye Diagram Tests 186
User Defined Real-Time Eye Diagram Test for Read Cycle Method of Implementation 189
User Defined Real-Time Eye Diagram Test for Write Cycle Method of Implementation 191

This section provides the Methods of Implementation (MOIs) for Custom Mode Read-Write Eye-Diagram tests using an Agilent 80000 or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR3 Compliance Test Application.

Probing for Custom Mode Read-Write Eye Diagram Tests

When performing the Custom Mode Read-Write Eye Diagram tests, the DDR3 Compliance Test Application will prompt you to make the proper connections as shown in Figure 53.

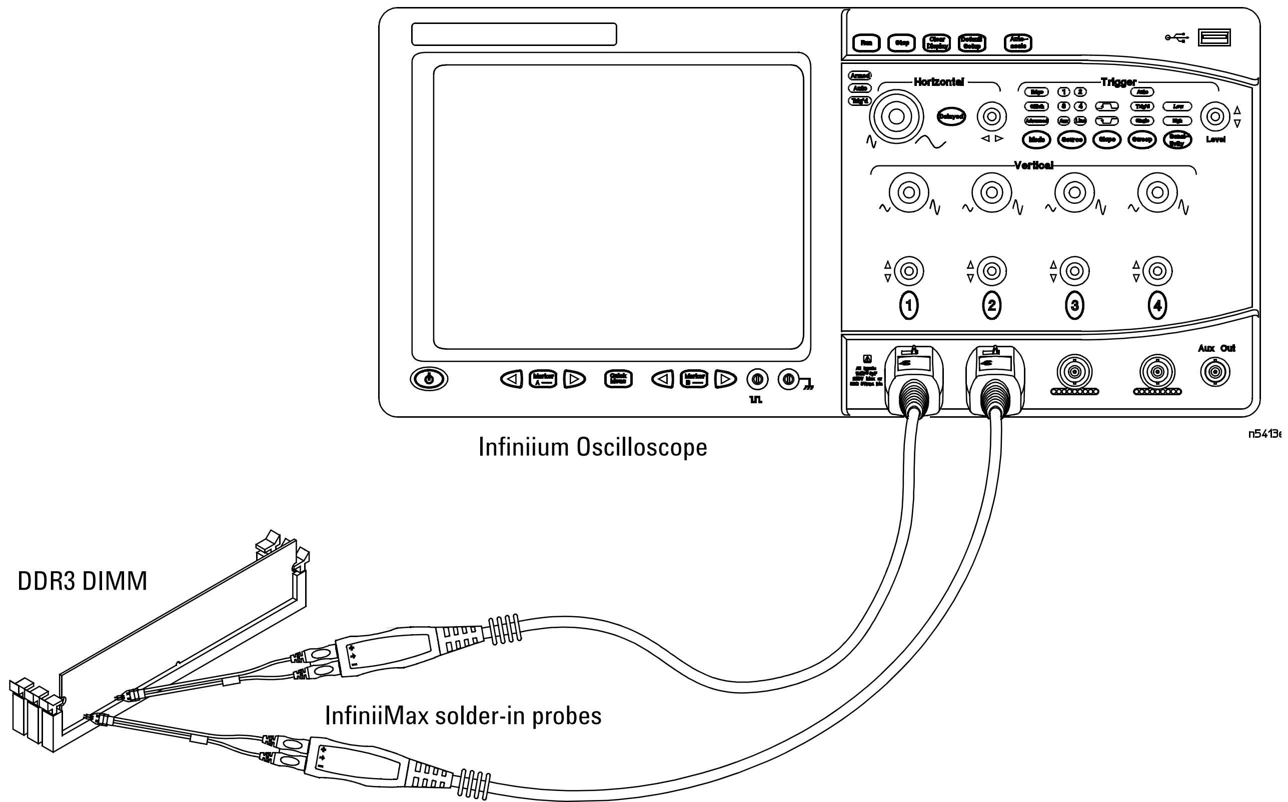


Figure 53 Probing for Custom Mode Read-Write Eye Diagram Tests

You can use any of the oscilloscope channels as the Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR3 Compliance Test Application. (The channels shown in Figure 53 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 13, “InfiniiMax Probing,” starting on page 209.

Test Procedure

1 Start the automated test application as described in "Starting the DDR3 Compliance Test Application" on page 25.

2 Ensure that the RAM reliability test software is running on the computer systems where the DDR3 Device Under Test (DUT) is attached. This software will perform a test on all the unused RAM on the system by producing repetitive bursts of read-write data signals to the DDR3 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR3 DIMM.

4 Connect the oscilloscope probes to any of the oscilloscope channels.

5 In the DDR3 Test application, click the Set Up tab.

6 Select Custom as the Test Mode option. This selection shows an additional command button - **Set Mask File**.

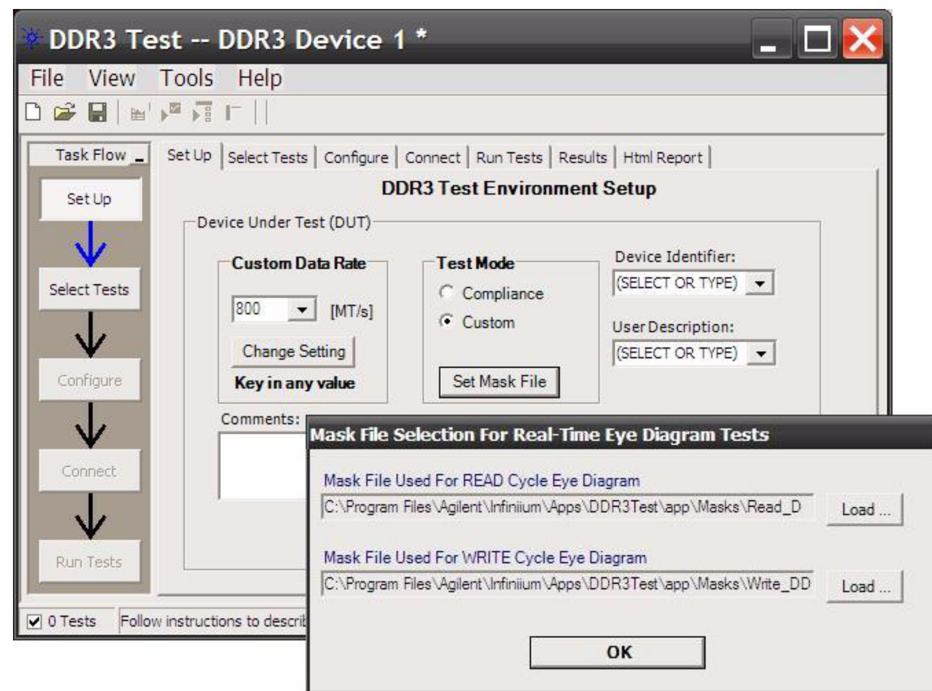


Figure 54 Selecting Custom Test Mode

7 Click this button to view or select test mask files for eye diagram tests.

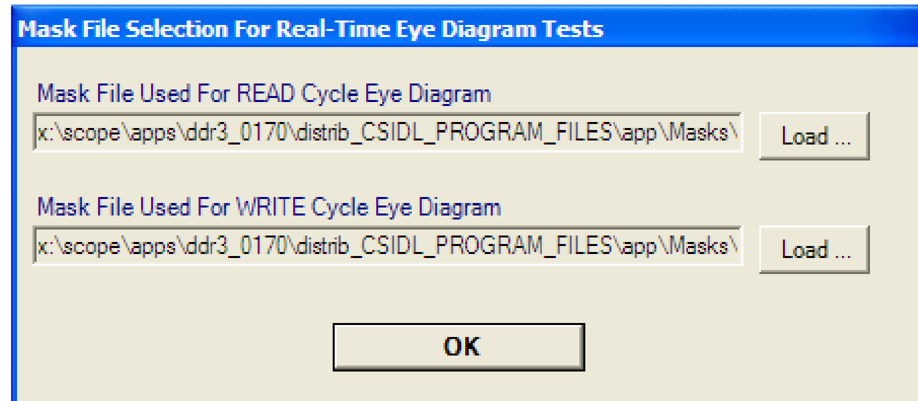


Figure 55 Selecting Test Mask for Eye Diagram Tests

8 Custom Mode also allows you to type in the data rate of the DUT signal.

9 Type in or select the Device Identifier as well as the User Description from the drop-down list. Enter your comments in the Comments text box.

10 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

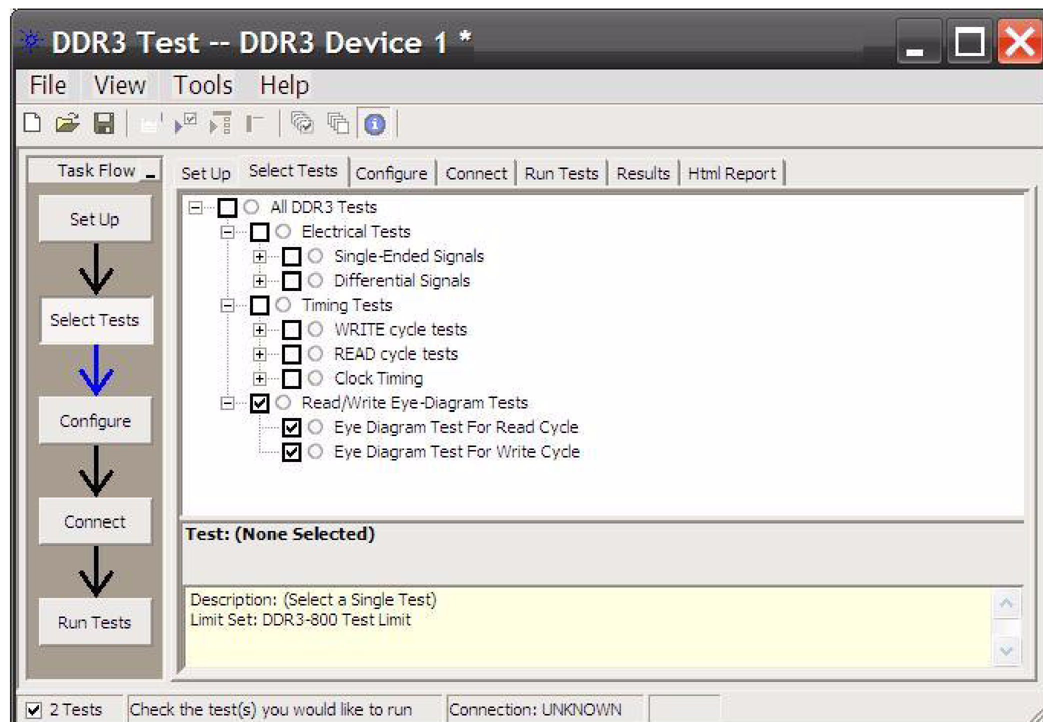


Figure 56 Selecting Custom Read-Write Eye-Diagram Tests

User Defined Real-Time Eye Diagram Test for Read Cycle Method of Implementation

The Custom Mode Read-Write Eye Diagram test can be divided into two sub-tests. One of them is the User Defined Real-Time Eye Diagram Test for Read Cycle. There is no available specification on the eye test in *JEDEC Standard JESD79-3* specifications. Mask testing is definable by the customers for their evaluation tests purpose. The purpose of this test is to automate all the required setup procedures in order to generate an eye diagram for the DDR3 data READ cycle. This additional feature of mask test allows you to perform evaluation and debugging on the created eye diagram. The test will show a fail status if the total failed waveforms is greater than 0.

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (supported by Data Strobe Signal)

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is DQ signals)
- Supporting Pin (only required when PUT is DQS)

Test References

There is no available test specification on eye testing in JEDEC specification. Mask testing is definable by the users for their evaluation tests usage.

PASS Condition

Generation of an eye diagram for the DDR3 data READ cycle and loading of a default test mask pattern.

Measurement Algorithm

1. Calculate initial time scale value based on selected DDR3 speed grade options.
2. Calculate number of sampling points according to the time scale value.
3. Check for valid DQS input test signals by verifying its frequency and amplitude values.

4 Set up the oscilloscope to generate an eye diagram.
   a Use UDF methodology to separate READ burst and return the filtered DQS signals as recovered clock for eye folding later.
   b Set up measurement threshold values for the DQx channel and the DQSx channel input.
   c Set up fix vertical scale values for DQx channel and DQSx channel input.
   d Turn on Color Grade Display option.
   e Identify the X1 value for re-adjustment of selected test mask.
   f Set up Mask Test settings.
   g Set up Clock Recovery settings on SDA.
   : Explicit clock, Source = DQS, Rise/Fall Edge
   h Turn on Real Time Eye on SDA.
5 Perform mask testing.
   a Set the termination condition of the mask test to ‘Waveforms’ with the number of waveforms to be acquired.
   b Start mask test.
6 Loop until the number of required waveforms is acquired.
7 Return the total number of failed waveforms as a test result.

User Defined Real-Time Eye Diagram Test for Write Cycle Method of Implementation

Just as in the previous test, there is no available specification on the eye diagram test in the *JEDEC Standard JESD79-3* specifications for User Defined Real-Time Eye Diagram Test for Write Cycle. Mask testing is definable by the customers for their evaluation tests purpose. The purpose of this test is to automate all the required setup procedures in order to generate an eye diagram for the DDR3 data WRITE cycle. This additional feature of mask test allows you to perform evaluation and debugging on the created eye diagram. The test will show a fail status if the total failed waveforms is greater than 0.

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (supported by Data Strobe Signals)

Signals required to perform the test on the oscilloscope:

- Pin Under Test (PUT is DQ signals)
- Supporting Pin (only required when PUT is DQS)

Test References

There is no available test specification on eye testing in JEDEC specification. Mask testing is definable by the users for their evaluation tests usage.

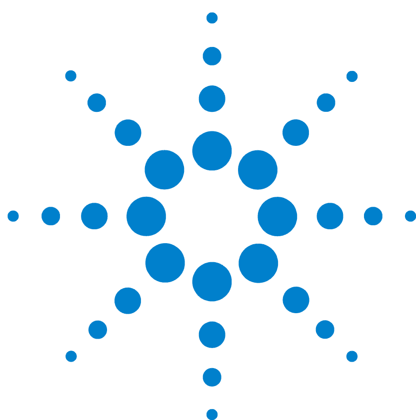
PASS Condition

Generation of an eye diagram for the DDR3 data WRITE cycle and loading of a default test mask pattern.

Measurement Algorithm

1. Calculate initial time scale value based on selected DDR3 speed grade options.
2. Calculate number of sampling points according to the time scale value.
3. Check for valid DQS input test signals by verifying its frequency and amplitude values.

4 Set up the oscilloscope to generate an eye diagram.
   a Use UDF methodology to separate WRITE burst and return the filtered DQS signals as recovered clock for eye folding later.
   b Set up measurement threshold values for the DQx channel and the DQSx channel input.
   c Set up fix vertical scale values for DQx channel and DQSx channel input.
   d Turn on Color Grade Display option.
   e Identify the X1 value for re-adjustment of selected test mask.
   f Set up Mask Test settings.
   g Set up Clock Recovery settings on SDA.
      : Explicit clock, Source = DQS, Rise/Fall Edge
   h Turn on Real Time Eye on SDA.
5 Perform mask testing.
   a Set the termination condition of the mask test to 'Waveforms' with the number of waveforms to be acquired.
   b Start mask test.
6 Loop until the number of required waveforms is acquired.
7 Return the total number of failed waveforms as a test result.



12
Calibrating the Infiniium Oscilloscope and Probe

Required Equipment for Oscilloscope Calibration 193
Internal Calibration 194
Required Equipment for Probe Calibration 197
Probe Calibration 198
Verifying the Probe Calibration 204

This section describes the Agilent Infiniium digital storage oscilloscope calibration procedures.

Required Equipment for Oscilloscope Calibration

To calibrate the Infiniium oscilloscope in preparation for running the DDR3 automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, Agilent p/n 54855-67604, qty = 2 (provided with the Agilent Infiniium oscilloscope).
- Calibration cable (provided with the 80000 and 90000A Series Infiniium oscilloscopes). Use a good quality 50 Ω BNC cable.

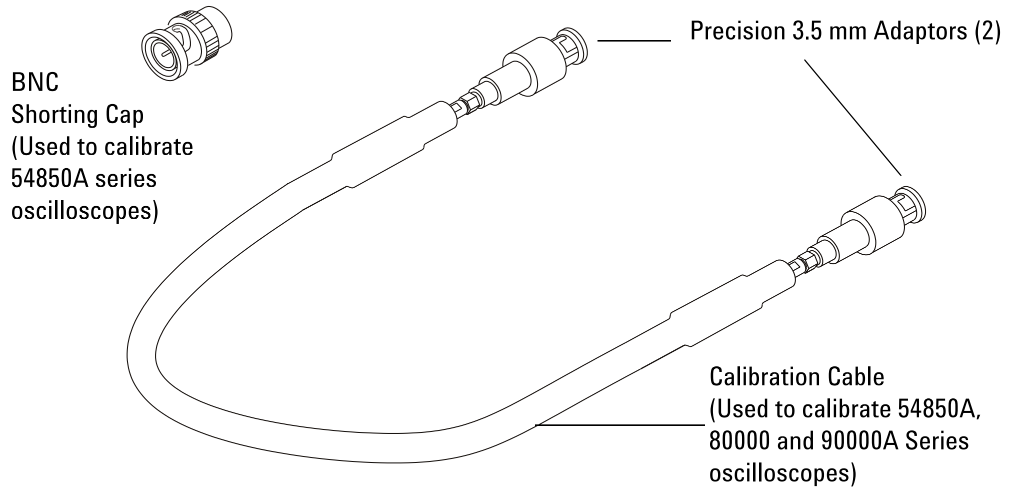


Figure 57 Accessories Provided with the Agilent Infiniium Oscilloscope

Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Agilent oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

1 Set up the oscilloscope with the following steps:

   a Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.

   b Plug in the power cord.

   c Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.

   d Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 3 below.

2 Locate and prepare the accessories that will be required for the internal calibration:

a Locate the BNC shorting cap.

b Locate the calibration cable.

c Locate the two Agilent precision SMA/BNC adapters.

d Attach one SMA adapter to the other end of the calibration cable - hand tighten snugly.

e Attach another SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to Figure 58 below, perform the following steps:

a Click on the Utilities>Calibration menu to open the Calibration dialog box.

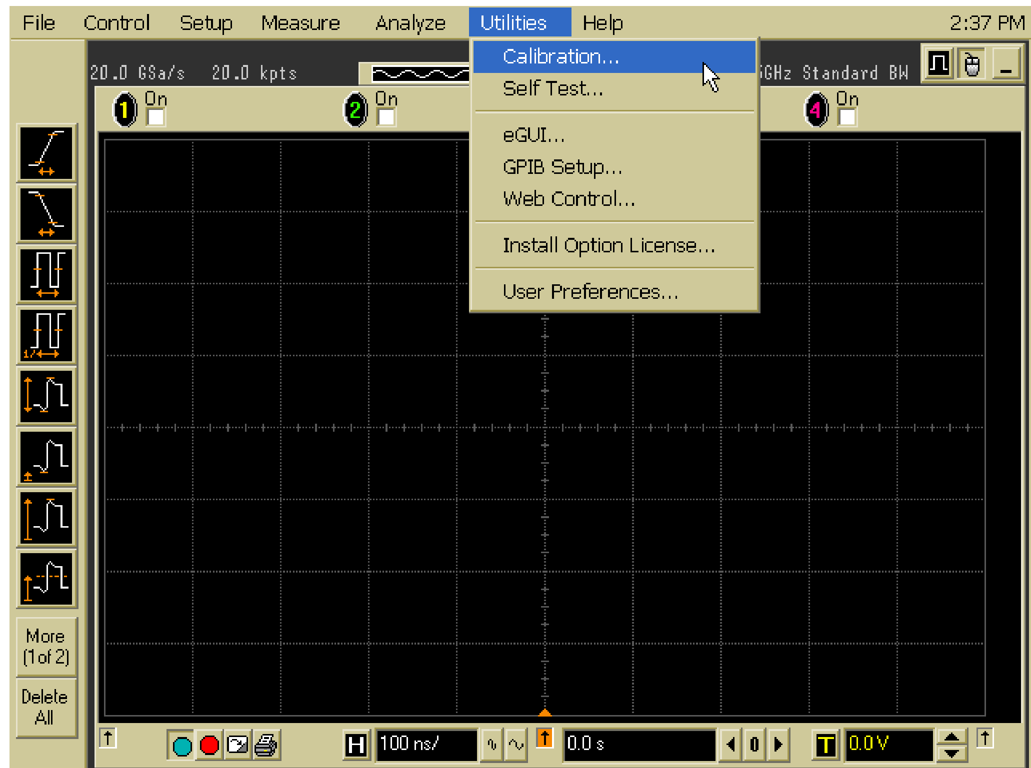


Figure 58 Accessing the Calibration Menu

4 Referring to Figure 59 below, perform the following steps to start the calibration:

b Uncheck the Cal Memory Protect checkbox.

c Click the Start button to begin the calibration.

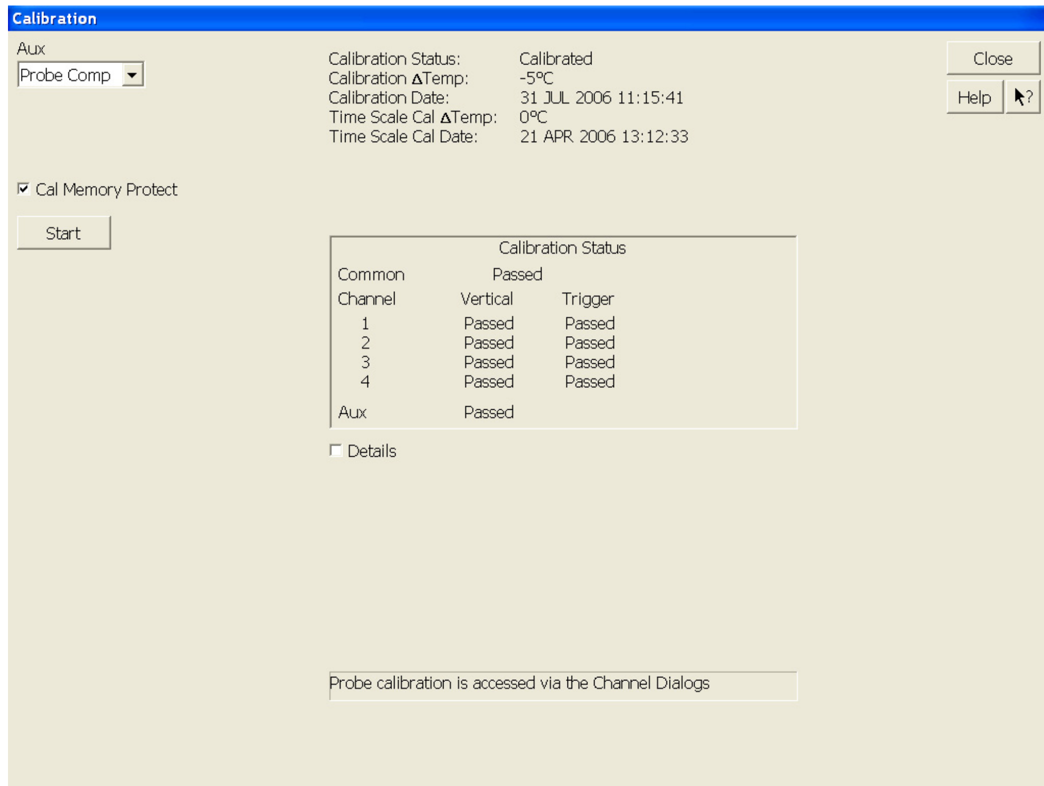


Figure 59 Oscilloscope Calibration Window

d During the calibration of channel 1, if you are prompted to perform a Time Scale Calibration, as shown in Figure 60 below.

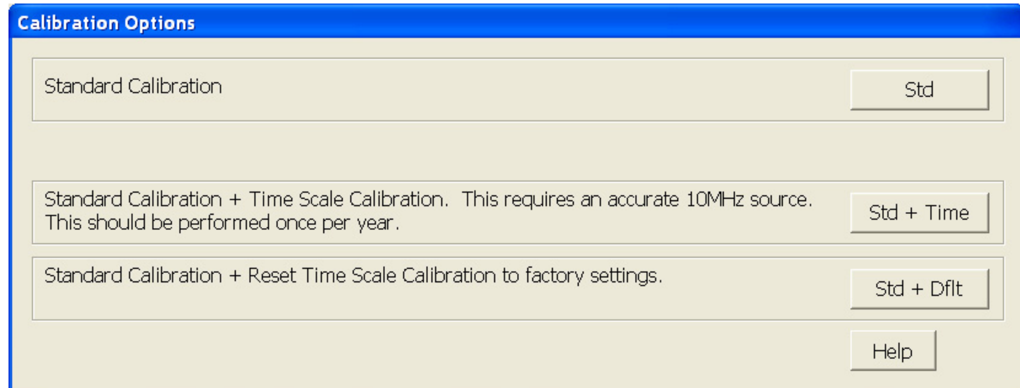


Figure 60 Time Scale Calibration Dialog box

e Click on the Std+Dflt button to continue the calibration, using the Factory default calibration factors.

f When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.

g Confirm that the Vertical and Trigger Calibration Status for all Channels passed.

h Click the Close button to close the calibration window.

i The internal calibration is completed.

j Read NOTE below.

NOTE

These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

Required Equipment for Probe Calibration

Before performing DDR3 tests you should calibrate the probes. Calibration of the solder-in probe heads consist of a vertical calibration and a skew calibration. The vertical calibration should be performed before the skew calibration. Both calibrations should be performed for best probe measurement performance.

The calibration procedure requires the following parts.

- BNC (male) to SMA (male) adaptor
- Deskew fixture
- 50 Ω SMA terminator

Probe Calibration

Connecting the Probe for Calibration

For the following procedure, refer to Figure 61 below.

1 Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.
2 Connect the 50 Ω SMA terminator to the connector farthest from yellow pincher.
3 Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.
4 Connect the probe to an oscilloscope channel.
5 To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.
6 Push down the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.
7 Release the yellow pincher.

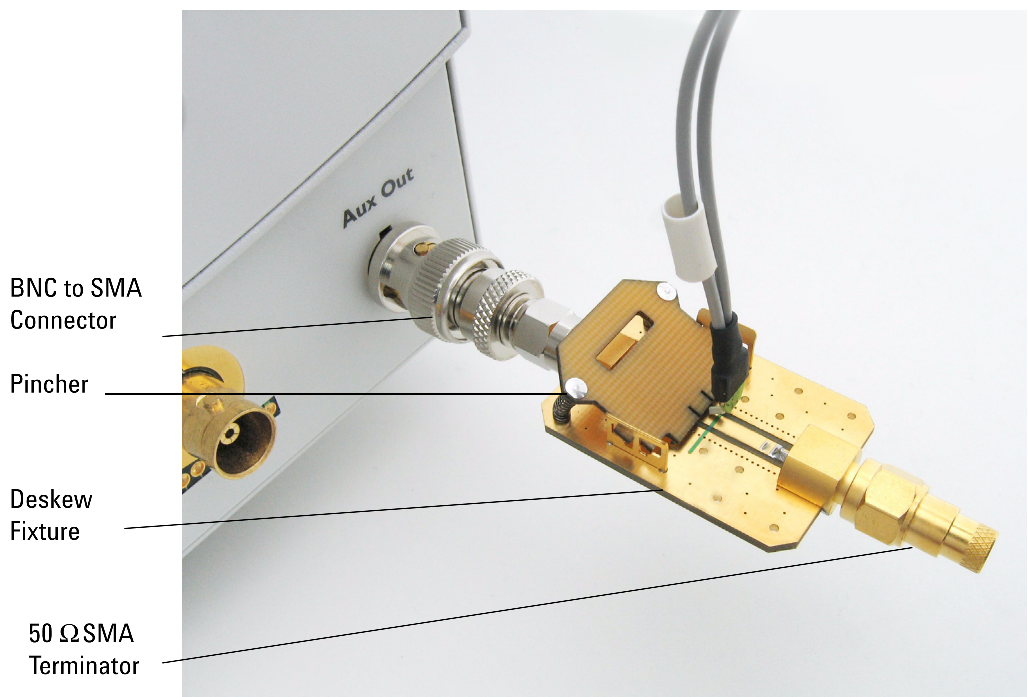


Figure 61 Solder-in Probe Head Calibration Connection Example

Verifying the Connection

1. On the Infiniium oscilloscope, press the autoscale button on the front panel.
2. Set the volts per division to 100 mV/div.
3. Set the horizontal scale to 1.00 ns/div.
4. Set the horizontal position to approximately 3 ns. You should see a waveform similar to that in Figure 62 below.

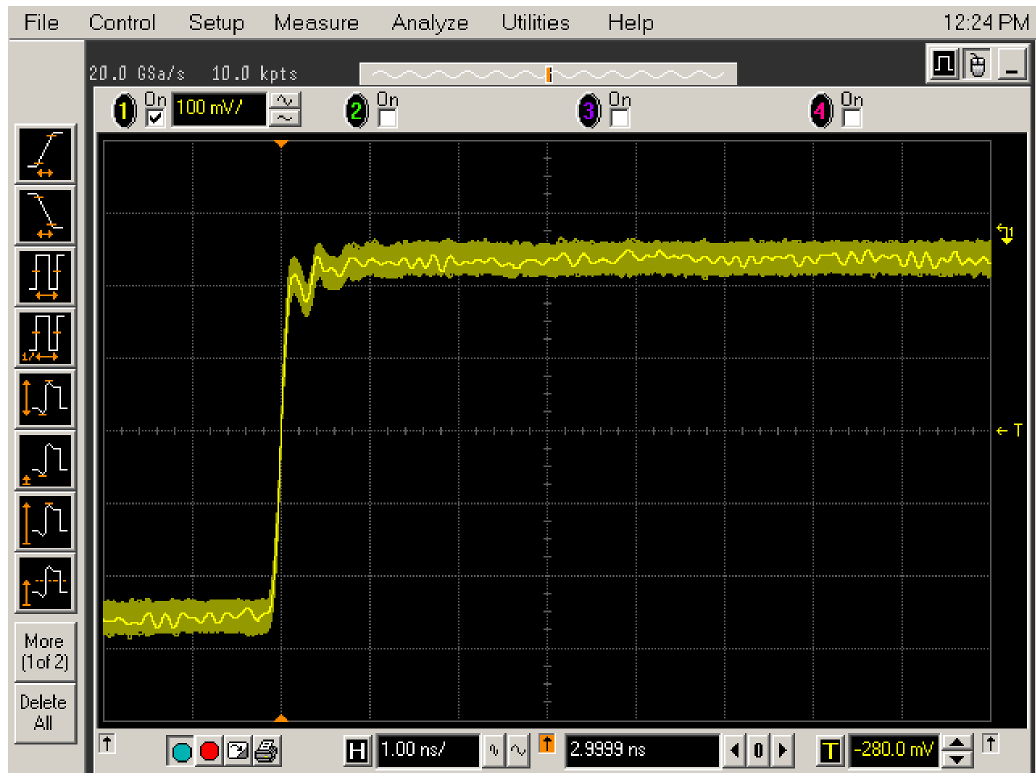


Figure 62 Good Connection Waveform Example

If you see a waveform similar to that of Figure 63 below, then you have a bad connection and should check all of your probe connections.

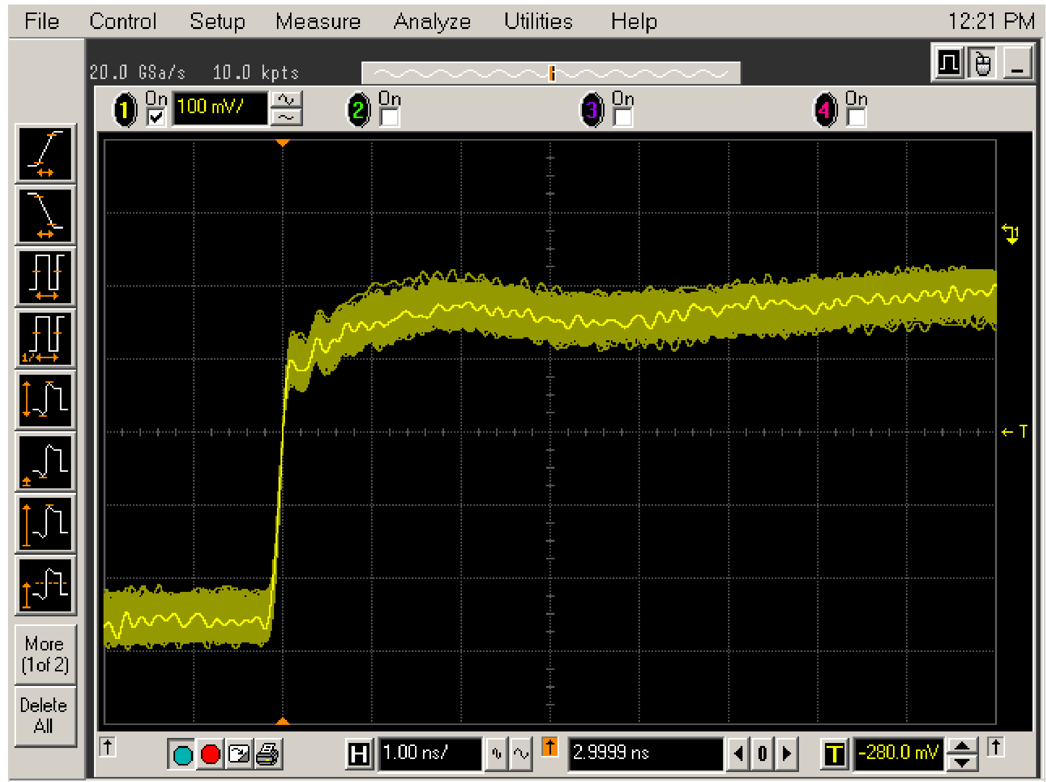


Figure 63 Bad Connection Waveform Example

Running the Probe Calibration and Deskew

1 On the Infiniium oscilloscope in the Setup menu, select the channel connected to the probe, as shown in Figure 64.

Figure 64 Channel Setup Window.

2 In the Channel Setup dialog box, select the Probes... button, as shown in Figure 65.

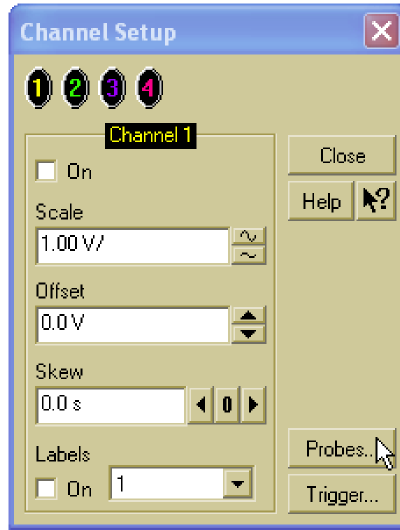


Figure 65 Channel Dialog Box

3 In the Probe Setup dialog box, select the Calibrate Probe... button.

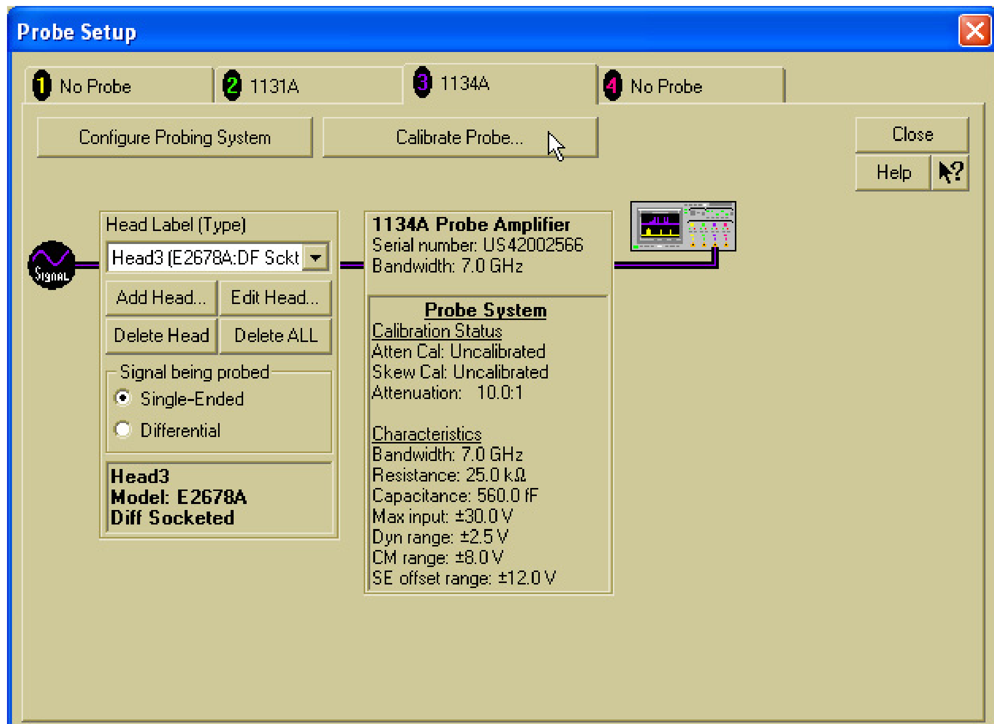


Figure 66 Probe Setup Window.

4 In the Probe Calibration dialog box, select the Calibrated Atten/Offset radio button.

5 Select the Start Atten/Offset Calibration... button and follow the on-screen instructions for the vertical calibration procedure.

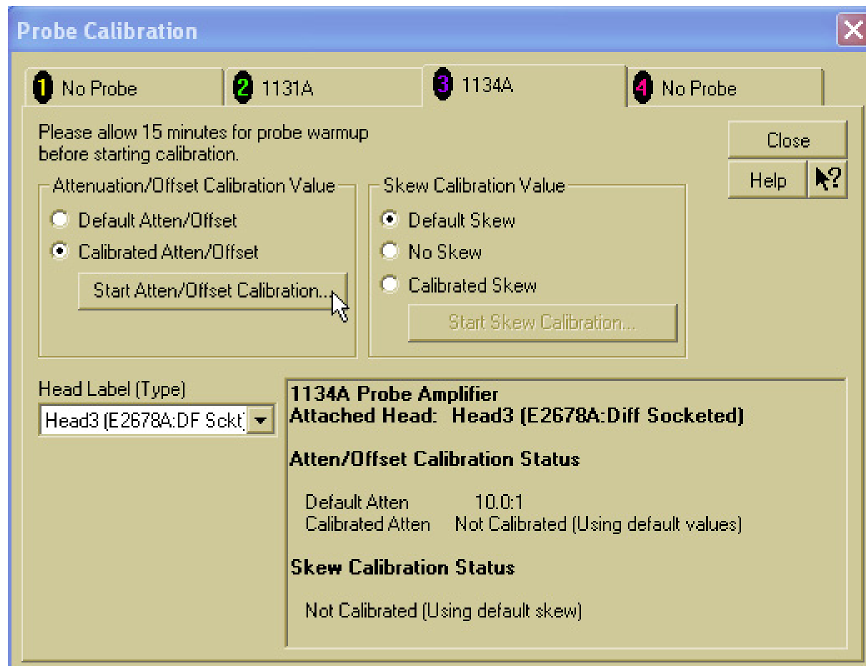


Figure 67 Probe Calibration Window.

6 Once the vertical calibration has successfully completed, select the Calibrated Skew... button.

7 Select the Start Skew Calibration... button and follow the on-screen instructions for the skew calibration.

At the end of each calibration, the oscilloscope will prompt you if the calibration was or was not successful.

Verifying the Probe Calibration

If you have successfully calibrated the probe, it is not necessary to perform this verification. However, if you want to verify that the probe was properly calibrated, the following procedure will help you verify the calibration.

The calibration procedure requires the following parts:

- BNC (male) to SMA (male) adaptor
- SMA (male) to BNC (female) adaptor
- BNC (male) to BNC (male) 12 inch cable such as the Agilent 8120-1838

- Agilent 54855-61620 calibration cable (Infiniium oscilloscopes with bandwidths of 6 Ghz and greater only)
- Agilent 54855-67604 precision 3.5 mm adaptors (Infiniium oscilloscopes with bandwidths of 6 Ghz and greater only)
- Deskew fixture

For the following procedure, refer to Figure 68.

1 Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.
2 Connect the SMA (male) to BNC (female) to the connector farthest from the yellow pincher.
3 Connect the BNC (male) to BNC (male) cable to the BNC connector on the deskew fixture to one of the unused oscilloscope channels. For infiniium oscilloscopes with bandwidths of 6 GHz and greater, use the 54855-61620 calibration cable and the two 54855-64604 precision 3.5 mm adaptors.
4 Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.
5 Connect the probe to an oscilloscope channel.
6 To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.
7 Push down on the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.
8 Release the yellow pincher.
9 On the oscilloscope, press the autoscale button on the front panel.
10 Select Setup menu and choose the channel connected to the BNC cable from the pull-down menu.
11 Select the Probes... button.
12 Select the Configure Probe System button.
13 Select User Defined Probe from the pull-down menu.
14 Select the Calibrate Probe... button.
15 Select the Calibrated Skew radio button.
16 Once the skew calibration is completed, close all dialog boxes.

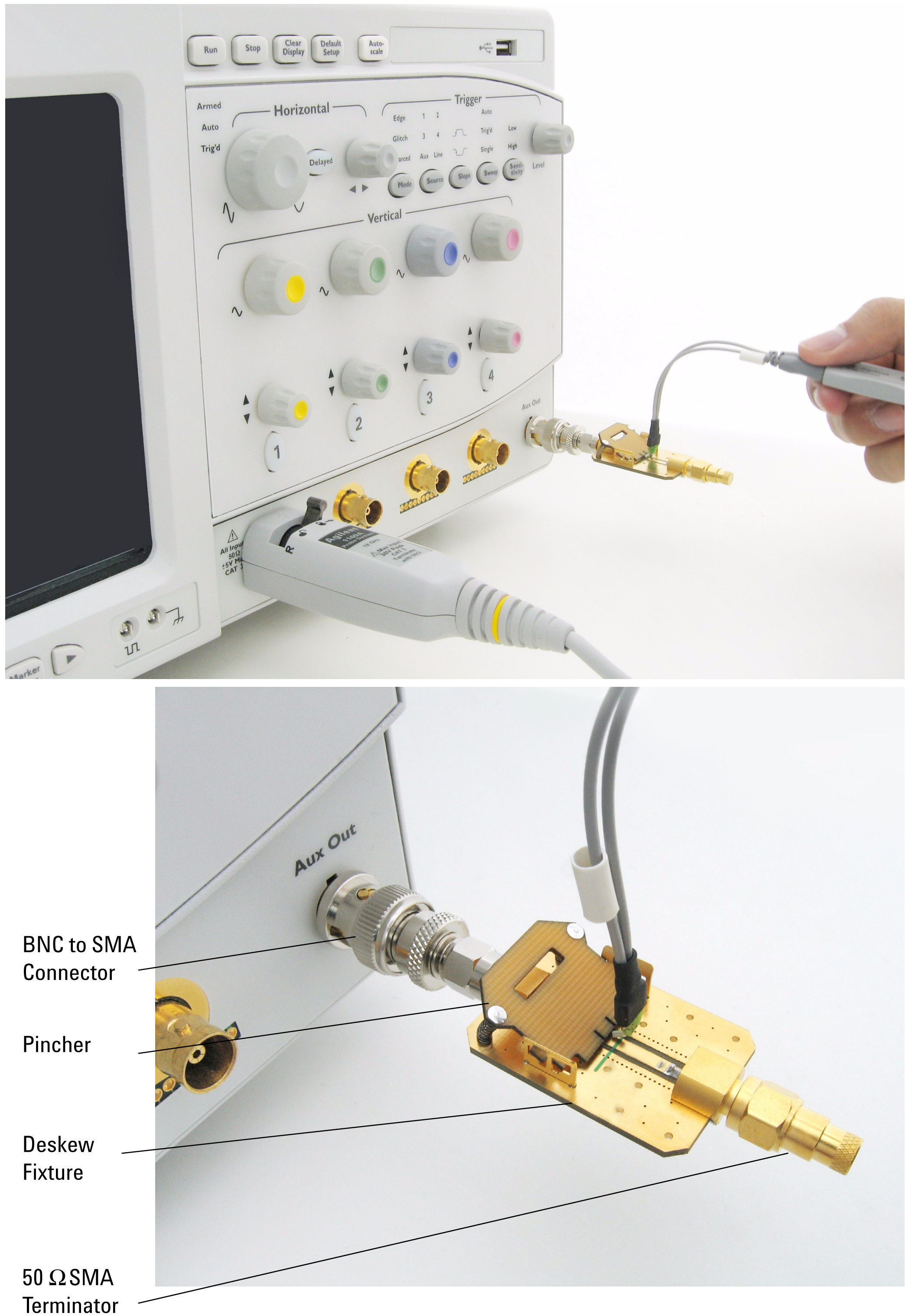


Figure 68 Probe Calibration Verification Connection Example

17 Select the Start Skew Calibration... button and follow the on-screen instructions.

18 Set the vertical scale for the displayed channels to 100 mV/div.

19 Set the horizontal range to 1.00 ns/div.

20 Set the horizontal position to approximately 3 ns.

21 Change the vertical position knobs of both channels until the waveforms overlap each other.

22 Select the Setup menu choose Acquisition... from the pull-down menu.

23 In the Acquisition Setup dialog box enable averaging. When you close the dialog box, you should see waveforms similar to that in Figure 69.

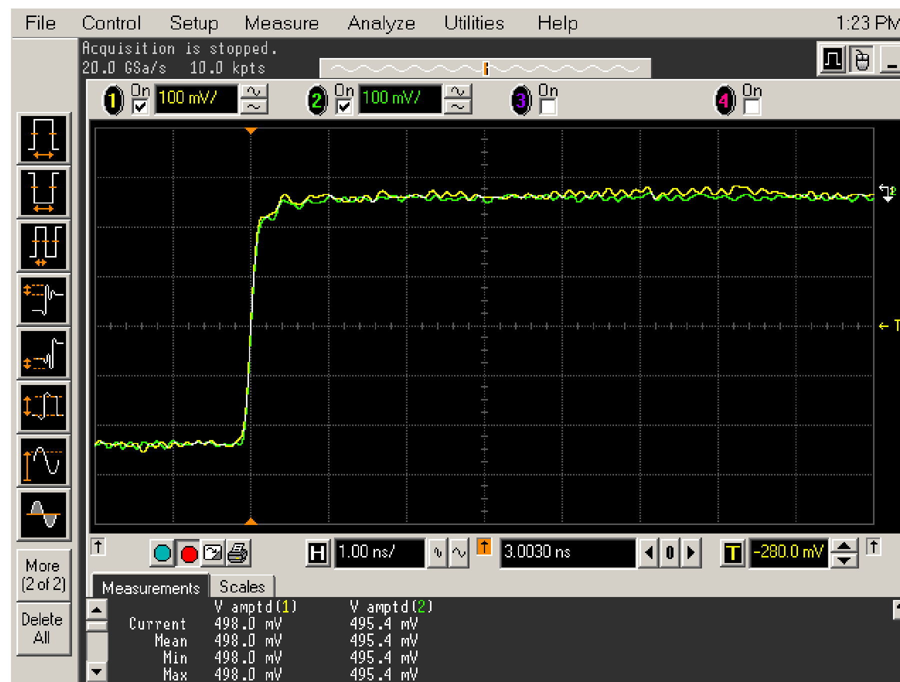


Figure 69 Calibration Probe Waveform Example

NOTE Each probe is calibrated with the oscilloscope channel to which it is connected. Do not switch probes between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the probes be labeled with the channel on which they were calibrated.

13
InfiniiMax Probing

Figure 70 1134A InfiniiMax Probe Amplifier

Agilent recommends 116xA or 113xA probe amplifiers, which range from 3.5 GHz to 12 GHz.

Agilent also recommends the E2677A differential solder-in probe head. Other probe head options include N5381A InfiniiMax II 12 GHz differential solder-in probe head, N5382A InfiniiMax II 12 GHz differential browser, E2675A InfiniiMax differential browser probe head, N5425A InfiniiMax ZIF probe head and N5426A ZIF Tips.

Figure 71 E2677A / N5381A Differential Solder-in Probe Head

Table 65 Probe Head Characteristics (with 1134A probe amplifier)

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential Solder-in	E2677A	7 GHz, 0.27 pF, 50 kOhm	7 GHz, 0.44 pF, 25 kOhm

Used with 1168A or 1169A probe amplifier, the E2677A differential solder-in probe head provides 10 GHz and 12 GHz bandwidth respectively.

Index

A

AC Differential Input Cross Point Voltage, 83
Address and Control Input Hold Time, 172, 180
Address and Control Input Setup Time, 169, 175
Average Clock Period, 103
Average High Pulse Width, 97
Average Low Pulse Width, 99

B

BNC shorting cap, 193
BNC to SMA male adapter, 193

C

calibrating the oscilloscope, 193
calibration cable, 193
Clock Timing (CT) Tests, 87
Clock to Clock Period Jitter, 92
computer motherboard system, 7
configure, 26
connect, 26
Cumulative Error, 94

D

Data Mask Timing (DMT) Tests, 133
Data Strobe Timing (DST) Tests, 107
differential browser, 7
Differential DQ and DM Input Hold Time, 140, 149
Differential DQ and DM Input Setup Time, 137, 143
differential solder-in probe head, 7, 209
DQ Low-Impedance Time from CK/CK#, 157
DQ Out High Impedance Time From CK/CK#, 155
DQ/DQS Output Hold Time From DQS, 162
DQS Falling Edge Hold Time from CK, 123
DQS Falling Edge to CK Setup Time, 120
DQS Input High Pulse Width, 116
DQS Input Low Pulse Width, 118
DQS Latching Transition to Associated Clock Edge, 114
DQS Low-Impedance Time from CK/CK#, 112
DQS Output Access Time from CK/CK #, 110
DQS-DQ Skew for DQS and Associated DQ Signals, 159

H

Half Period Jitter, 101
HTML report, 26

I

in this book, 8
InfiniiScan software license, 7
Input Signal Minimum Slew Rate (Falling), 36
Input Signal Minimum Slew Rate (Rising), 33
internal calibration, 194

K

keyboard, 7, 193

L

license key, installing, 21

M

Maximum AC Output Logic High, 61
Maximum DC Input Logic Low, 48
Maximum DC Output Logic Low, 67
Minimum AC Input Logic Low, 48
Minimum AC Output Logic Low, 65
Minimum DC Input Logic High, 42
Minimum DC Output Logic High, 63
mouse, 7, 193

O

Output Logic High Test, 61
Output Logic Low High Test, 65
Output Signal Minimum Rising Slew Rate (Falling), 58
Output Signal Minimum Rising Slew Rate (Rising), 55
over/undershoot tests, 69

P

precision 3.5 mm BNC to SMA male adapter, 193
probe calibration, 198
Probing for Advanced Debug Mode Read-Write Eye Diagram Tests, 186
Probing for Clock Timing Tests, 88
Probing for Command and Address Timing Tests, 166
Probing for Data Mask Timing Tests, 134
Probing for Data Strobe Timing Tests, 108
Probing for Differential Signals AC Input Parameters Tests, 80
Probing for Overshoot/Undershoot Tests, 70
Probing for Single-Ended Signals AC Input Parameters Tests, 30
Probing for Single-Ended Signals AC Output Parameters Tests, 52

R

RAM reliability test software, 7
Read Cycle, 189
Read Postamble, 131
Read Preamble, 129
report, 26
required equipment and software, 7
required equipment for calibration, 193
results, 26
run tests, 26

S

select tests, 26
Serial Data Analysis and Clock Recovery software license, 7
SlewF, 36
SlewR, 33
SRQseF, 58
SRQseR, 55
start the DDR3 Compliance Test Application, 25

T

tCH(avg), 97
tCK(avg), 103
tCL(avg), 99
tDH(base), 140, 149
tDQSCK, 90
tDQSH, 116
tDQSL, 118
tDQSQ, 159
tDQSS, 114
tDS(base), 137, 143
tDSH, 123
tDSS, 120
tERR(n per), 94
tHZ(DQ), 110
tIH(base), 172, 180

tIS(base), 169
tJIT(cc), 92
tJIT(duty), 101
tJIT(per), 90
tLZ(DQ), 157
tLZ(DQS), 112
tQH, 161, 162
tRPRE, 129
tRPST, 131
tWPRE, 127
tWPST, 125

U

User Defined Real-Time Eye Diagram Test, 189, 191

V

VID(AC), 83
VIH(ac), 39
VIH(dc), 42
VIL(ac), 45
VIL(dc), 48
VIX(ac), 83
VOH(AC), 61
VOH(DC), 63
VOL(AC), 65
VOL(DC), 67

W

Write Cycle, 191
Write Postamble, 125
Write Preamble, 127

Z

ZIF probe, 7
ZIF tips, 7